SONY

Training Manual

KD-34XBR2

KDP-57XBR2

Direct View & Projection TVs

HA-3/RA-5A Chassis

Models: KD-34XBR2
KDP-57XBR2
KDP-65XBR2

Troubleshooting Information

Course: CTV-29/TVP-12 (C29P12)

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Introduction

This training manual covers circuit description and troubleshooting for the direct view HA-3 TV chassis and the similar projection TV RA-5A chassis. This information is on two levels. The first level covers board replacement. As you read further, you enter the second level containing the information for component level to repair the board. When repairing at component level, references are made to the DTV-02 training manual (P/N = DTV021000), which contains circuitry similar to the HA-3 direct view TV circuitry.

Models Covered

Model numbers related to the HA-3 and RA-5A chassis are listed in Chart 1-1:

Chart 1-1 - Related Model Number	
HA-3 Chassis Direct View TV Models	RA-5A Chassis Projection TV Models
KD-34XBR2	KDP-57XBR2
	KDP-65XBR2

The "D" in the model name refers to the digital decoder box built into the TV that can decode the 18 ATSC digital TV formats approved for the USA and Canada over the air transmission. ATSC stands for "Advanced Television Standards Committee" and replaces the 1940 NTSC (National Television Standards Committee) standard. The above models have a 16 x 9 aspect ratio screen in compliance with most of the ATSC formats.

Chart 1-2 – TV Inputs	
Video	Off the Air / Cable
Video 1-4 – 480i NTSC format	Air – NTSC channels 2-69
Video 5-6 – 480i NTSC format or 480p, 720p, 1080i ATSC format	Air – ATSC channels 2-69
	Cable – NTSC channels 1-125

Technical Highlights

- There are three microprocessors in the Q box and the TV operations micro is on the B board. They are listed in Chart 1-3 below:

Chart 1-3 – Microprocessors in the TV		
Q box (DTV decoder)	B Board	AD Board
Digital Processor	Main TV Micro	Convergence Micro (PJ TV only)
MPS CPU (i LINK)		
MID Microprocessor		

- The Q box micros talk to the TV micro using separate receive (RXD) and transmit (TXD) lines. The Main TV Micro talks to the TV ICs using the standard I^2C communications format.
- The New white OSD Menu is generated by one of the Q box micros.
- The TV micro generates the service mode OSD and green displays as before but there are two intensities for the green channel display. When changing channels, the green channel number shows at full intensity for 1.5 seconds then drops in brightness to prevent burning the CRT.
- All the video passes through the Q box. The Q box is exchanged as a package.
- There are self-diagnostics in these TV sets with memory to assist in locating shutdown causes.
- One horizontal high scan frequency of 33.75kHz, yields less geometry/convergence adjustments.
- Geometry / Convergence Adjustments are made in the FULL picture mode and its data is copied into most other picture modes

- There are three power supplies in each of these TV sets. The primary supply must start before the secondary supply operates, and the horizontal sweep must be active before the HV power supply becomes active.
- There is no filament preheating from the primary power supply as in the similar Sony ® model KV32XBR400 (DX-1A chassis). The CRT filament voltage comes from the HOT.
- There are only a few mechanical adjustments in these TV sets and they are listed in Chart 1-4 below:

Chart 1-4 - Mechanical Adjustments	
Direct View TV (HA-3 chassis)	Projection TV (RA-5A chassis)
G2 (screen) – C board	G2 (screen) controls - chassis
H Static control – C board	Static electrical focus - chassis
Static focus on the Flyback - D board	Mechanical focus - lenses
HV reg. and shutoff point (2 epoxy sealed controls) – D board	HV reg. and shutoff point (2 epoxy sealed controls) – D board

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New Features

Menu

The video, screen mode and setup menus are new or have changed. The changes to the menu are explained below:

Video Menu

Refer to Figure 2-1 for a sample of the video menu.

Video	
Picture Mode	Vivid
Picture	
Brightness	
Color	
Hue	
Sharpness	
Color Temperature	Cool
VM	High
DRC Mode	CineMotion
Alternate Video	Alternate 1

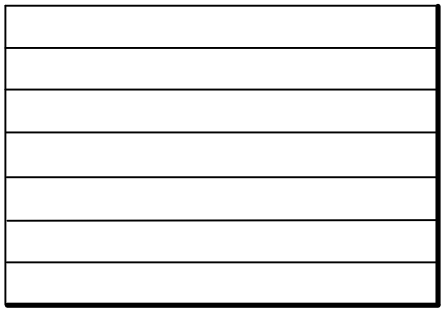
Figure 2-1

DRC Mode = Interlaced / Progressive / CineMotion – There are three choices offered in the DRC mode. The Digital Reality Creation (DRC) module within the Q box converts the NTSC input video to a higher resolution picture. This is necessary so a standard resolution input can be presented on this high-scan TV screen. During the conversion, you can instruct the DRC module to output the high-resolution video in one of three modes: Interlaced, Progressive or CineMotion.

Interlaced picture is for moving images – A single TV frame consists of two picture fields (see Figure 2-2). Each field contains on half of the picture and was originally presented this way in the NTSC TV standard to reduce flicker.

"6i" Interlaced Picture consisting of alternating lines from fields 1 & 2

Figure 2-2 - Interlaced Pix



"6p" Progressive Scan Picture

Figure 2-3 - Progressive Pix

Progressive picture is for still pictures – When the TV screen contains pages of still text or a still image, an interlaced picture appears to jitter. This is because field 2 displays the same picture as field 1, but is positioned lower. When the fields are displayed one after the other, a still picture appears to jump. The solution is to not displace these lines (see Figure 2-3). Progressive scan only has one field per picture so a still image does not jump.

CineMotion is for movies shot at 35mm or wide 70mm – Movie film is NOT shot at the same rate that television presents a picture. A Telecine Conversion must take place to present the 24 frames/sec of movie film in the 30-frames/sec (60-fields/sec) TV rate. This conversion is also referred to as 3:2 pulldown because the first frame is duplicated three times and the second twice (see Figure 2-4) before repeating. The result is that sometimes two different film picture frames are merged into an interlaced TV frame. As a result, there may not be smooth movement. Therefore, this Telecine conversion distorts moving TV images.

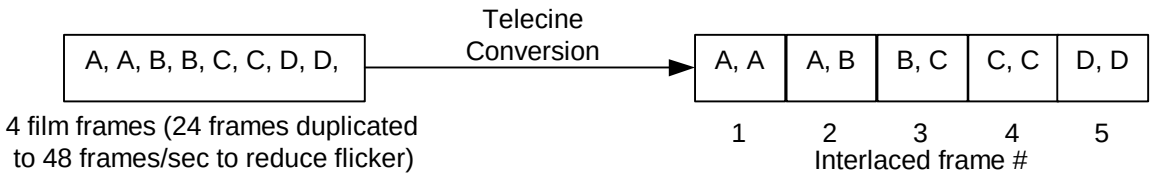
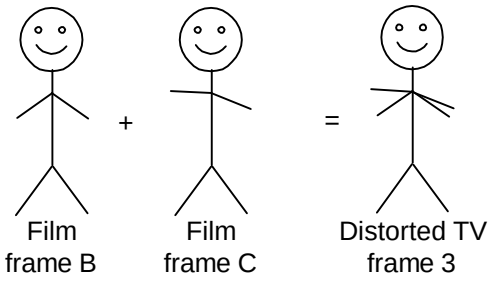

A, A, B, B, C, C, D, D,
Telecine Conversion
A, A
A, B
B, C
C, C
D, D
4 film frames (24 frames duplicated to 48 frames/sec to reduce flicker)
1 2 3 4 5
Interlaced frame #

Figure 2-4 - CineMotionProblem



The distortion is eliminated in this TV's CineMotion mode by restoring the original film sequence, eliminating the 3:2 pulldown originally used for timing (see Figure 2-5). Each TV frame contains the same picture so the movie is clearer. The time difference between film and TV video is compensated for by digitally storing and displaying the movie frames for a longer period.

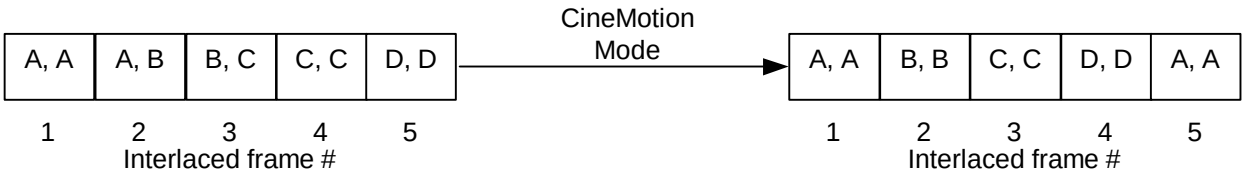


Figure 2-5 CineMotion Solution

Alternate Video / Audio - Refer to Figure 2-1 for a sample menu page. If this feature in the DTV transmission is available, the user can select a second video or audio stream for a different camera angle or second language.

Screen Modes Menu

Refer to Figure 2-6 for a sample Screen Mode menu.

Screen Mode	
Wide Mode	Wide Zoom
4:3 Default	Off
Vertical Center	
Vertical Size	

Figure 2-6 - Screen Mode Menu

Wide Mode - you can alter the 4:3 picture you are watching into:

Wide Zoom – The sides of a 4:3 picture are stretched while the top and bottom are condensed.

Normal – No change to the 4:3 picture.

Full – The 4:3 picture is just stretched horizontally.

Zoom – The 4:3 picture is enlarged to maintain aspect ratio.

4:3 Default - Allows the TV to enter one of the above Wide Modes when you change stations. If "OFF" is selected, the 4:3 picture will remain in the size selected by Wide Mode.

Setup Menu

Refer to Figure 2-7 for a sample setup menu page.

Select Out - Selects Monitor for the same screen pix, TV for tuner, or Video 1-4 regardless of what you are watching.

i Link Setup - Allows you to select a product like a cable box, which is connected to the rear panel i Link (IEEE1394) jack.

i Link Standby - Allows the TV to remain at a power level between standby and ON so an i Link device can power this TV ON.

Vertical Correction - Vertical position (centering)

Factory Reset – Clears all user settings and the active TV channels found so only channels 2-13 are loaded. The TV shuts off momentarily and loads the defaults at turn ON.

Setup	
Caption Vision	Off
Select Out	Monitor
Video Input	
Language	
i Link Setup	
i Link Standby	Off
Set Clock/Timers	
Vertical Correction	
Tilt Correction	
Demo	
Factory Reset	

Figure 2-7 - Setup Menu

i LINK ®

i Link ® and Fire Wire ® are trade names for the IEEE-1394 high-speed communications standard that can support digital video, audio and data. It uses transaction-based packet technology to communicate between devices. This standard was developed to help bridge the gap between PCs and consumer electronic products.

Compatibility

The purpose of i Link is to transmit and receive high-speed data. The data may include digital audio and video data as well as communications data in the ideal arrangement. In this early i Link acceptance stage, no digital video or audio input is possible with this TV. Communications with this TV is limited to operation with the Sony CableVision cable box currently used in NYC. Therefore, the following information shows how to connect i LINK devices and what this TV does with an i LINK connected device.

Connection for Speed

The IEEE-1394 allows the data transmission speed to vary between devices, but the proper connection will improve communications speed. In Figure 2-8, the PC or scanner would have no trouble communicating with the camcorder at a rate of 100 Mb/s. However, the scanner could not communicate with the PC at its top data rate of 200 Mb/s because the path between the two contains a 100 Mb/s device (the camcorder). The maximum data rate that can be achieved through another device is limited to the speed of that device.

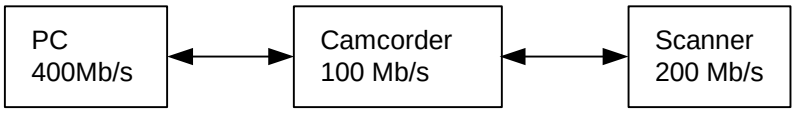


Figure 2-8 - Bandwidth limited by slower device

In Figure 2-9, the PC and the scanner would be able to communicate at the scanner's top rate of 200 Mb/s. It is important that when an IEEE-1394 network is set up, that high-speed devices are connected to high-speed devices and lower speed devices are placed at the end of the chain.

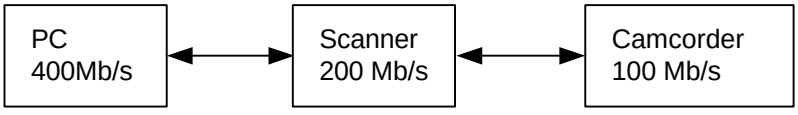


Figure 2-9 - Improved Hookup

The rear panel i Link connectors on the back of this TV (see Figure 2-10) connect to hardware and software in the DTV's "Q box" to identify and react with other i Link devices. The speed of this i Link device is marked next to the connector as 200 Mb/s.

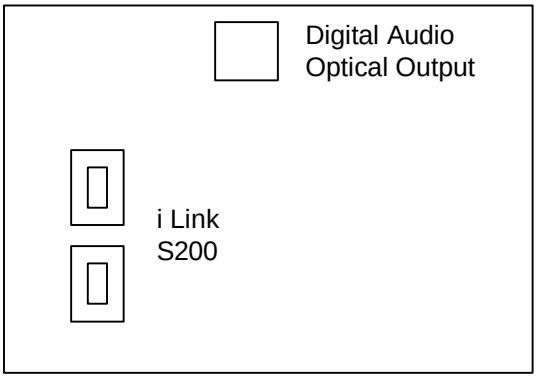


Figure 2-10 - Back panel of TV

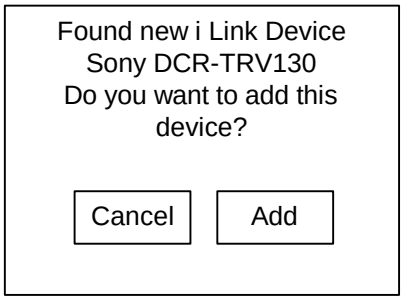


Figure 2-11 - TV screen after i Link connection

Operation

Once another i Link device is connected and turned on, communications occurs. The DTV displays the message shown in Figure 2-11 at the center of the screen. When you select "Add", a second message may appear if the digital inputs formats are compatible. The message will ask you to select the input for this i Link device. Afterwards a momentary message says the setup is now complete. You can now press the i Link button on the front panel or remote and see the new i Link device listed along with the DTV i Link device itself. Whenever you select that device from the list, the two will operate together. In this example, the output of Sony camcorders is a digital DV format. The DTV set is expecting an MPEG digital video format and therefore cannot display the DV format video on the screen. An analog cable between the two is needed to display the camcorder video as explained in the owner's manual. The TV's video 1 input must then be selected manually to view the camcorder picture.

i Link Circuitry

The i Link circuits and jacks are at the rear of the QI board. The four pins of each i Link jack (CN9203 and CN9294) are connected to eight individual pins of IC9203 (see Figure 2-12 for the circuitry). The QI circuitry is provided as reference since both QI and QM boards are replaced as an assembly.

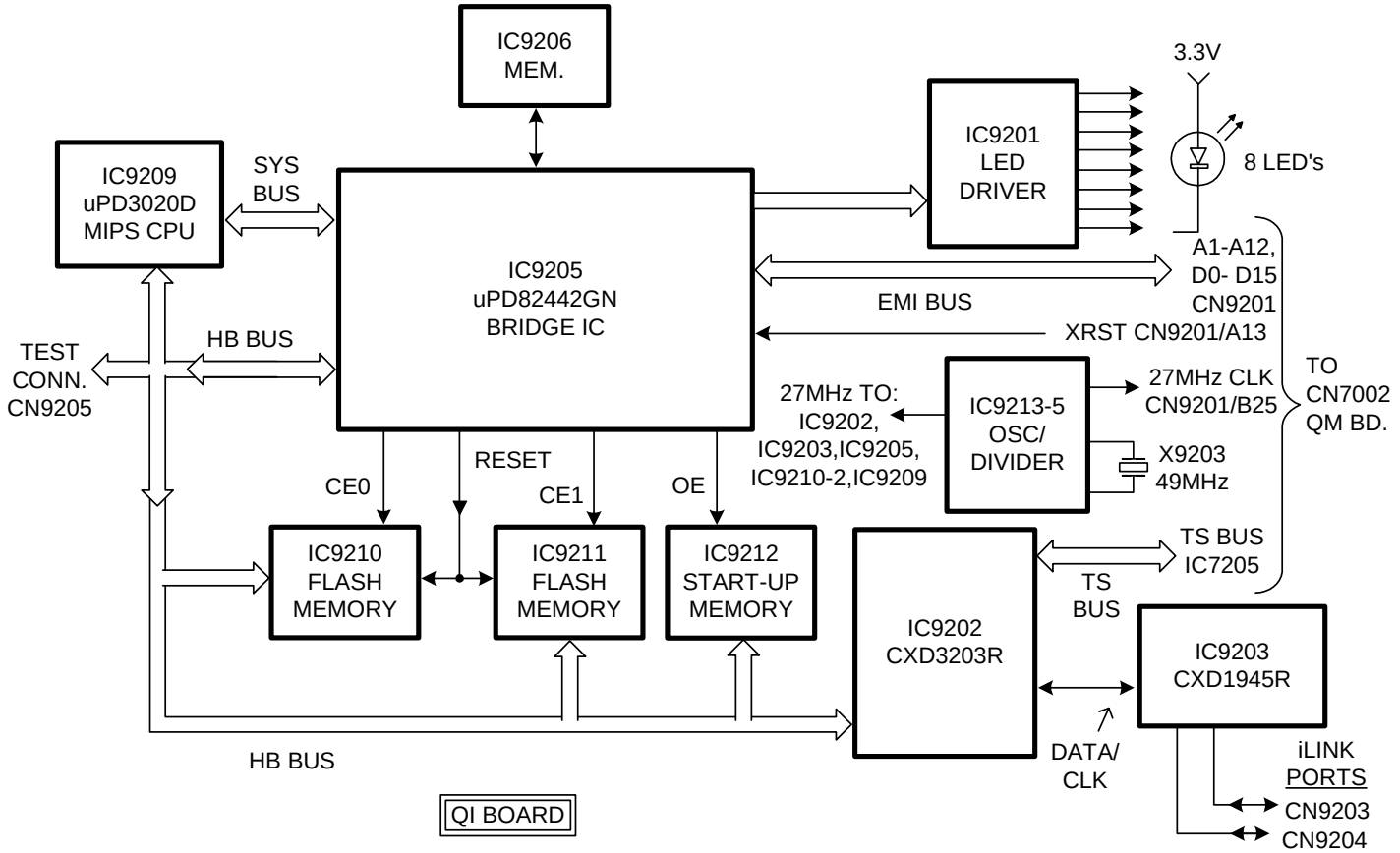


FIGURE 2-12 - iLINK CIRCUITRY

1TVP12 1319 9/4/01

The microprocessor for the i Link program is IC9209, but the i Link data is stored in upgradable Flash memory IC9210 and IC9211. IC9205 is an IC that acts as an interface or bridge to another micro IC7205 (not shown) on the QM board via the EMI bus. This bridge is necessary because the B+ for these two ICs are different so the HB bus and EMI bus are at different voltage levels. This often occurs in new design to match ICs. Bridge IC9205 also acts as an expansion IC using SYS bus to perform driver (output) functions such as Output Enable (OE) for start up data.

IC7205 (not shown) communicates with the main micro (B board) in the TV and contains the i Link OSD graphics that are routed to OSD IC8801.

The eight LEDs and IC9201 driver are used in i Link software loading verification (not for servicing). The left LED with the rear of the QI board facing you is the reset LED for the board. It lights up at reset. Reset occurs shortly at power ON and just before the memory stick information gets processed.

Fire Wire® is a trademark of Apple Computer Inc.
i Link® is a trademark of Sony.

DTV Signal Information

Digital TV Transmissions

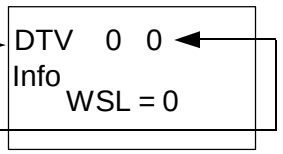
In addition to receiving the current channel 2-69 NTSC format TV stations and channel 01-125 cable stations, these TV sets contain an extra tuner to receive off-the-air channel 01-99 Digital stations in the ATSC format. DTV channels 01-99 are mostly in the UHF band because the channel 2-13 VHF band is currently occupied with analog NTSC stations.

During this transition period as the USA and Canada move from the current analog NTSC format to the digital ATSC format, transmitting stations will be sending out both formats on two different channels. Some of the current DTV transmissions are of low power to lower their operating costs of a second transmitter and the programming is duplicated with sporadic HDTV transmissions. By now (2001), all major networks have DTV transmissions in the larger cities.

Signal Contents

You can determine the noise level and contents of the DTV signal being received by going to the service mode and examining the transmitted PSIP information received by the TV's decoder:

1. Enter the service mode: Using the remote control, press buttons: Display, 5, Volume +, Power On.
2. Select an active DTV station using the channel up/down buttons.
3. Use the 2 (up) or 5 (down) buttons to locate category DTV.
   The WSL indicates signal strength like AGC. 0 = strong and 255 = snow.
4. Use the 3 or 6 buttons to change the data from 0 to 1.
5. Information about the received channel (similar to Figure 3-1) will be added to the screen from the Q box.



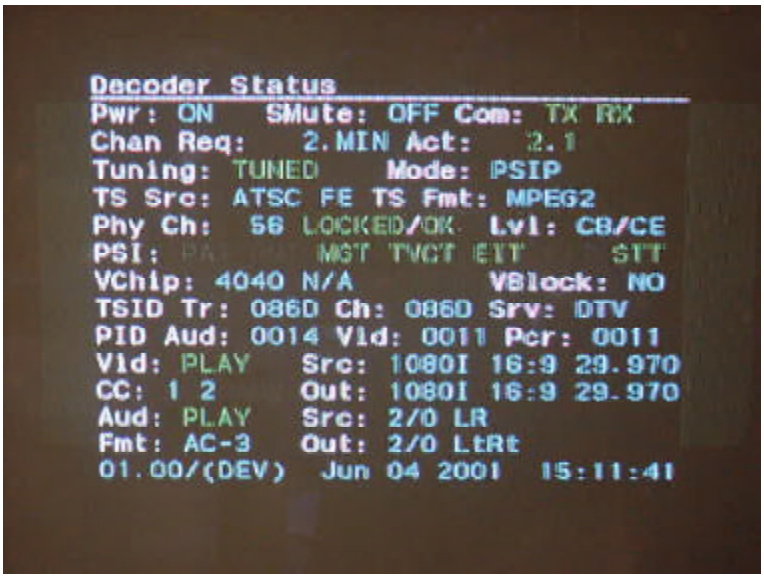

Decoder Status
Pwr: ON SMute: OFF Com: TX RX
Chan Req: 2.MIN Act: 2.1
Tuning: TUNED Mode: PSIP
TS Src: ATSC FE TS Fmt: MPEG2
Phy Ch: 56 LOCKED/OK Lvl: CB/CE
PSI: PAT MGT TVCT EIT STT
VChip: 4040 N/A VBlock: NO
TSID Tr: 086D Ch: 086D Srv: DTV
PID Aud: 0014 Vid: 0011 Pcr: 0011
Vid: PLAY Src: 1080I 16:9 29.970
CC: 1 2 Out: 1080I 16:9 29.970
Aud: PLAY Src: 2/0 LR
Fmt: AC-3 Out: 2/0 LtRt
01.00/(DEV) Jun 04 2001 15:11:41

Figure 3-1
DTV Signal Information

Contents of the DTV Signal

The Decoder Status page as pictured in Figure 3-1 reveals that:

- The DTV received channel is UHF channel (Phy Ch) 56, but the channel number displayed on the TV screen is (Act) 2.1.
- The digital video decoding is (Fmt) MPEG2 and the audio decoding is (Fmt) AC-3.
- Closed caption (CC) levels 1and 2 are being sent
- The transmitted resolution is (Video Src) 1080i in the 16:9 aspect ratio.
- Although the audio decoding requested is AC-3, a 6-channel system, there are only two front channels encoded and no (0) rear channels sent (Audio Src: 2 / 0 LR).

Signal Quality

You can also determine the quality of the received signal while still in the service mode. If the digital signal is correct, the decoder will process the information and output audio and video in sync. If there are sunspots, rain, or airplanes for example that can distort the signal the decoder will take longer to try to resolve the errors. Therefore, the time the signal enters and leaves the decoder will be longer. This delay identifies digital reception errors.

You can see the audio and video processing time in the service mode. From the service mode, select category DTV. Use the remote's number 3 button to change the data from 1 to 3.

The following audio and video data packet processing example shown in Figure 3-2 shows the packet number going into the TV's decoder (PTS) and what packet has been successfully processed (PCR). At the right is the decoder processing time is given in ms. The greater the difference in packet number or processing time in ms, the poorer the signal quality (since the decoder takes longer to try to resolve digital errors). A large number of digital errors may be due to sunspots, airplanes, storms or transmission errors. The picture shown in Figure 3-2 is of a good quality signal.

Figure 3-2
Input/Output
Packet data

HA-3 Chassis Overall Block

The HA-3 TV chassis is the first direct view TV that contains a DTV decoder. This decoder is identified as the "Q" box and is a shielded assembly within the TV. Currently only the KD-34XBR2 model houses the HA-3 chassis. The major stages of the model KD-34XBR2 bridge several boards as shown in Figure 4-1. These stages are:

- Power supply (A, D and F boards)
- Video Processing Stage (B board)
- Deflection Stages (described in detail within the DTV-02 training manual) (D board)

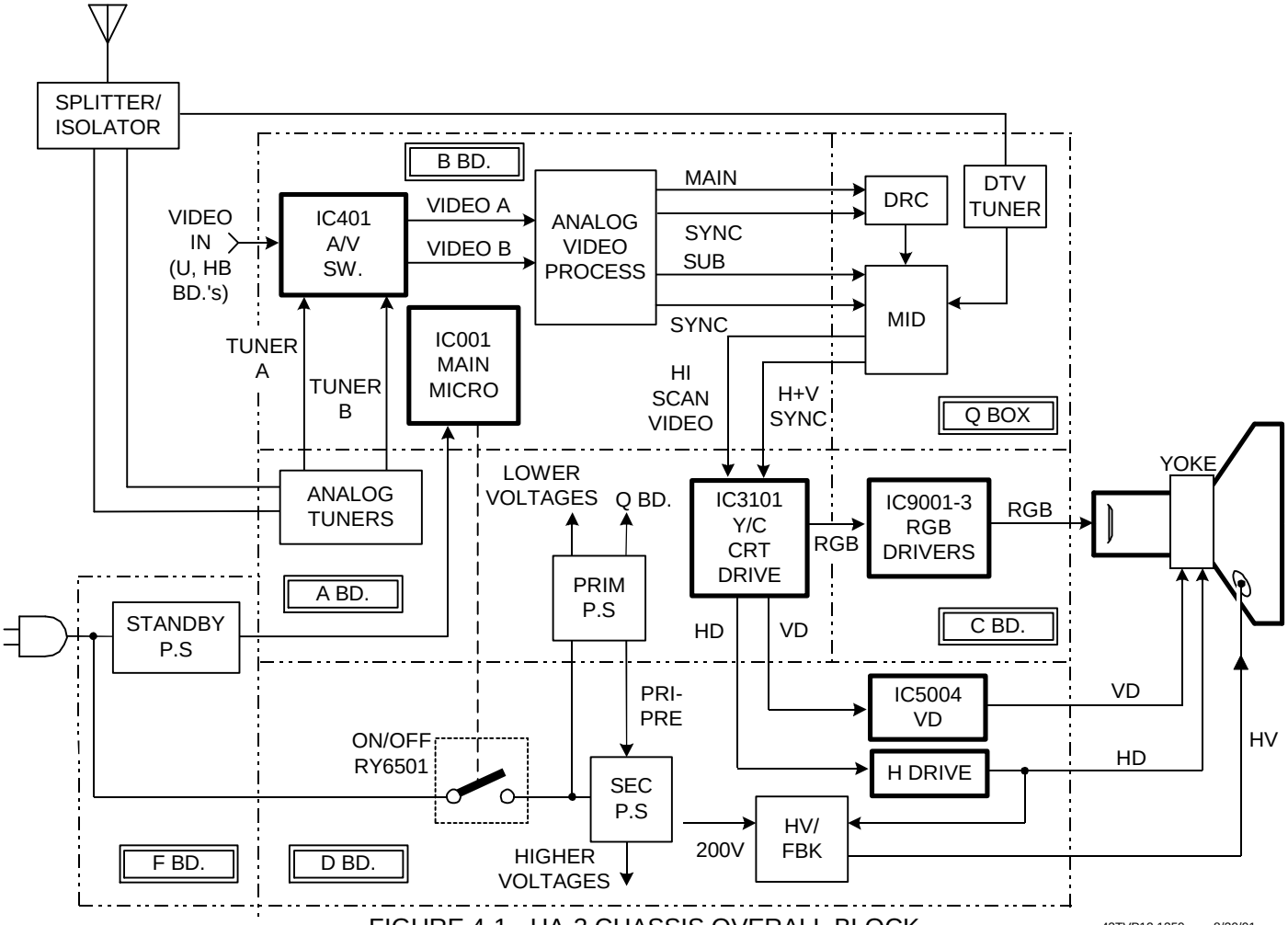


FIGURE 4-1 - HA-3 CHASSIS OVERALL BLOCK 43TVP12 1359 8/30/01

Power Supply

The power supply consists of three parts as shown in Chart 4-1:

Chart 4-1 - Model KD34XBR2 / HA-3 Chassis Power Supplies		
Name	Board	Purpose
Standby	F	Powers Main Micro IC001 and AC relay. Outputs Standby 7 and 15Vdc
Primary	A	Outputs 12Vdc and lower voltages to the A, B and S boards. Outputs Pri-Pre 15V to start the Secondary Power Supply.
Secondary	D	Supplies the deflection (D) board with the higher voltages such as 200V (HV), 135V (H Defection), and 24V (audio).

The Primary power supply starts the secondary supply using a Pri-Pre 15V line. Once the Secondary power supply operates, these voltages supply the deflection circuitry on the D board and the HV starts.

Video Processing

This TV will accept standard resolution inputs or high-resolution inputs.

Standard Resolution Input – A standard resolution signal could be selected from either analog tuner (NTSC) or any composite video 1-4 input. However, this high resolution TV runs at a different horizontal frequency of 33.75kHz than what is input. To view a standard NTSC signal (480i) that runs at 15,734 Hz on this TV, the video signal must be improved and the horizontal sync more than doubled. The improvement is performed in the DRC circuits and the sync conversion and picture sizing is done in the MID circuitry. Both of these circuits are part of the Q box.

The Digital Reality Creation (DRC) Circuit analyzes each pixel of a line to add another line. Therefore, the DRC circuit doubles the number of video lines of a standard NTSC signal. The DRC also doubles the horizontal sync frequency before passing the signal onto the MID circuit on the same board.

The Multi Image Driver (MID) Circuit stores the lines and outputs the signal based on a new horizontal frequency that matches the TV. At the higher frequency, the picture finishes before the scan. Blank lines are added as filler by this MID stage before leaving the board.

The output of the Q box is a "Hi-Scan" (high-resolution) picture with separate H & V sync lines that are applied to the Y/C CRT Drive IC3101 (A board). IC3101 converts the component video input into RGB for the CRT cathodes and uses the sync input to lock the 60 Hz vertical oscillator and 33.75kHz horizontal oscillator.

High Resolution Input - Video inputs 5 and 6 are for Y, Pr and Pb component video signal types only. They can be standard (480i) or high resolution (480p, 720p or 1080i) formats. The standard resolution signal must be switched into the DRC circuit using the Main path (for up conversion), and the high-resolution signals must be sent into the MID circuit using the Sub path (for sizing and sync conversion).

The DTV tuner signal is also fed into the MID circuit (Q box). The MID circuit selects one input (or two of the inputs when in the Twin mode) and outputs a single "Hi Scan" picture with corrected sync to match the 33.75kHz TV frequency. The component video that outputs the Q box is applied to Y/C CRT Drive IC3101 on the A board. This IC level shifts (matrixes) the signal into an RGB output signal for each CRT cathode.

Deflection Stages

Chart 4-2 shows the two stages that feed the deflection yoke.

Chart 4-2 – HA-3 Chassis Deflection Stages – D board

Stage	Drive Source	Power Supply	Diagnostic Indication
Vertical Sweep	Y/C CRT Drive IC3101	± 15Vdc from the Secondary PS (D Bd)	Blinks 4X
Horizontal Scan	Y/C CRT Drive IC3101	+135Vdc from the Secondary PS (D Bd)	Blinks 2X, 3X, or 7X

Vertical Sweep – Vertical drive signal comes from Y/C CRT Drive IC3101 synced to signal from the MID circuitry on the QM board (in the Q box).

Horizontal Scan - Y/C CRT Drive IC3101 also develops H drive signal. The H drive is not only used to drive the yoke, but also starts the HV Regulator stage.

HA-3 Chassis - Power ON Block

Power Supplies

There are four power supplies in the HA-3 direct view TV chassis. These are listed in Chart 5-1 below:

Chart 5-1 - Model KD32XBR2 – HA-3 Chassis Internal Power Supplies			
Name	Board	Start	Purpose
Standby	F	AC Plug in	5V for Main Micro 7V & 15V for power relay
Primary	A	Power ON (Voltage from AC Relay RY6501)	Unreg 11V, 7V, 5V become regulated 9V, 5V, 3.3V.
Secondary	D	Primary Pre 15V, Main Relay (5V)	+200V for HV stage, +135V for H. Output, ±15V, +24V for Audio stage *
HV Converter (not shown)	D	Horiz Output AFC-PLS (5Vp-p)	31.5kV HV for CRT, Focus voltage.

* see Chart 5-4 for the destination of output voltages

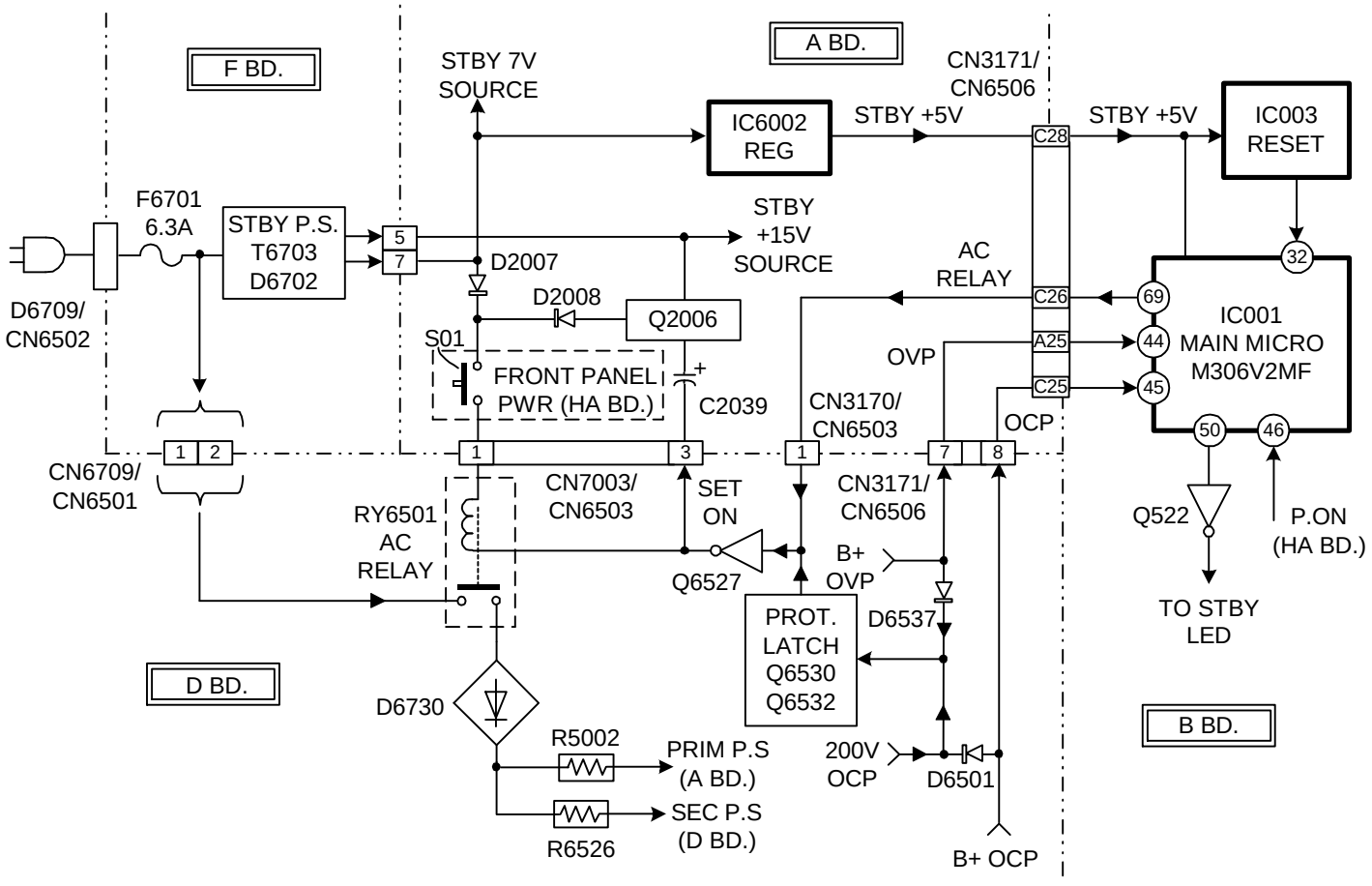


FIGURE 5-1 - POWER ON 1/2 12TVP12 1330 8/30/01

Except for the Standby power supply, the Primary, Secondary and HV Converter supplies are similar. The last three supplies use the same IC in a similar configuration. They differ in how they are turned ON and their output voltages.

Each power supply is turned ON in the order listed. The standby power supply is operational when the TV is plugged into AC. When the TV is powered ON, the second and third supplies are turned ON one after the other. These supplies power the horizontal stages. Finally, the fourth (HV) power supply is turned ON after the horizontal output transformer develops scan (AFC pulses are used). The HV power supply is not shown on Figure 5-1, but knowing when the HV is powered ON is important for troubleshooting.

Standby Power Supply

When the TV is plugged in, the standby power supply outputs three voltages: +15V, +7V and +5V. A small transformer develops the +15V and +7V. The +7V is regulated down to +5V to power the Main MicroIC001.

Primary & Secondary Power Supplies

Before power ON can occur, the front panel master ON/OFF button (S01 on the HA board) must be pressed in. This latching switch behind the button supplies the AC relay (RY6501) with standby 7V. Pressing the switch again would unlatch the switch and the set would shut OFF.

Power ON can be activated either from the remote control or when the front panel button is latched in. The second half of front panel switch S01 (not shown) grounds the power ON input to Main Micro IC001. IC001 powers ON the TV by turning on relay driver Q6527. Q6527 grounds one end of RY6501 relay coil and momentarily turns on Q2006 via C2039. Q2006 supplies a higher +15V to AC relay RY6501 because a relay requires more voltage to close the contacts than to hold them closed, especially if the AC input voltage is below normal at that time. Once RY6501's contacts close, D6730 is powered and 340V is applied to the Primary and Secondary power supplies.

Primary Power Supply

Starting

This primary power supply only needs 340Vdc from the bridge rectifier D6530 to start up and run.

Output Voltages

The Primary Power Supply outputs low voltages labeled "Sub" and "Q" voltages. The Q voltages go to the Q box and the Sub voltages are distributed to the TV for operation. The Sub and Q voltages may be checked at the board's connector as shown in Chart 5-2.

Chart 5-2 – Primary Power Supply Output Voltage Checkpoints

Output	Checkpoint	Output	Checkpoint
Sub 12V	CN6002/pin 1	Q6.5V	CN6005/pin 1, 2
Sub 9V	CN4402/pin 7 or CN3020/pin C4, C5	Q9V	CN6005/pin 6
Sub 5V	CN3020/pin C6, C7	Q5V	CN6005/pin 5
Sub 3.3V	CN3020/pin C2, C3		

The most important output voltage from the primary power supply is the "Pri Pre 15V" output. This volume starts the Secondary power supply on the D board.

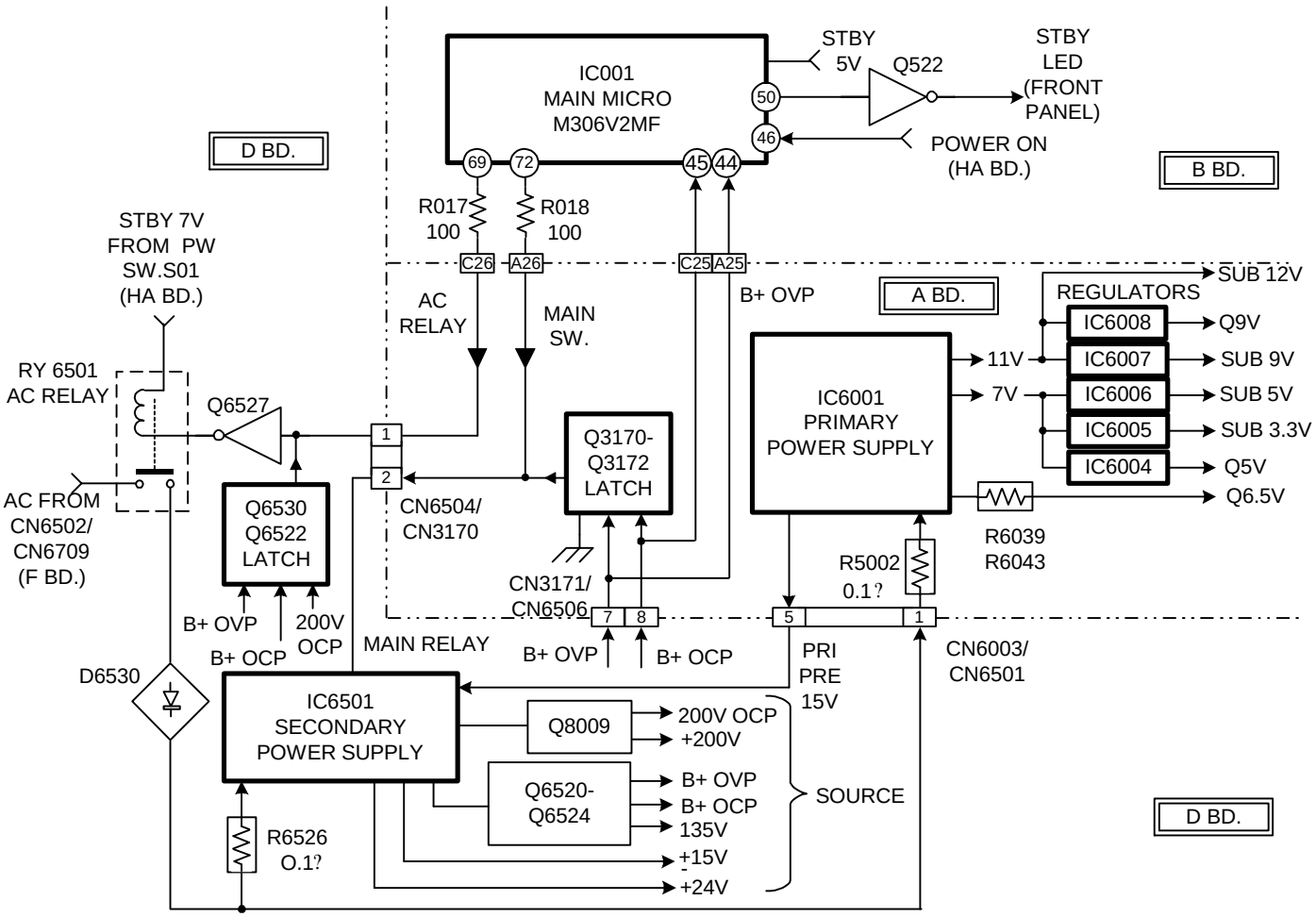


FIGURE 5-2 - DIAGRAM 13 - POWER ON 2/2

13TVP12 1331 8/30/01

Secondary Power Supply

Starting

The Secondary Power Supply needs three items to operate. They are listed in Chart 5-3 below:

Chart 5-3 - Three voltages needed to run the Secondary Power Supply		
Item	From	Purpose
1. 340Vdc (B+)	Bridge Rectifier D6530	Powers the Driver/Output
2. Pri Pre 15V voltage	Primary Power Supply's secondary winding	Starts the oscillator when above 15.6Vdc.
3. Main Relay (normally HIGH)	Main Micro IC001	Enables IC6501 when HIGH

Output Voltages

This secondary power supply produces the remainder of the low voltages to power the TV. These are listed in Chart 5-4.

Chart 5-4 - Secondary Power Supply Load		
Output	Protected	Destination
200V	Yes OCP	D Board - HV Converter power supply
135V	Yes. OVP, OCP	D board - Horizontal stages Sample voltage returned for regulation
+24V	No	D board - Makes Main 12, Main 9 and Main 5V used throughout the D board *
+15V	No	A board - Audio output stage

* see Chart 5-1 for source of voltages

TV Power ON Sequence

1. Press the PWR ON button;
2. AC Relay energizes (RY6501);
3. Primary Power Supply starts (Q box is powered, Surge relay is energized);
4. Main Micro (B board) resets Q box (The Q box has flash memories for self initialization);
5. Q box acknowledges after initializing (TXD and RXD communications. See appendix);
6. Main Micro (B board) starts the Secondary Power Supply (Deflection and TV filaments start). The Secondary power supply is started 100msec after power ON and independent of the Q box acknowledgment (step 5);
7. Main Micro (B board) retrieves information from the NVM ICs on the B communications bus and sends the data to the appropriate TV operating ICs using the S communications bus;
8. HV starts after horizontal deflection operates (D board);
9. Shutdown circuitry is enabled (B board); and
10. IK circuitry (A board) adjusts the gain of the RGB amplifiers and unmutes the RGB signal to the CRT.

Primary Power Supply (HA-3 & RA-5A Chassis)

The Primary and Secondary power supplies are similar in operation. They differ in schematic nomenclature (component numbers) and output voltages. The HA-3 simplified secondary power supply is shown in Figure 6-1 for this description.

The primary power supply on the HA-3 chassis A board consists of three parts:

1. Oscillator 2. Output stage 3. Regulator Stage

The oscillator starts up to produce an initial signal for the output stage. The output stage develops voltage to continue running the oscillator stage, supply the regulating stage, and provide normal output for the TV. One of the normal TV outputs is used to start the secondary power supply.

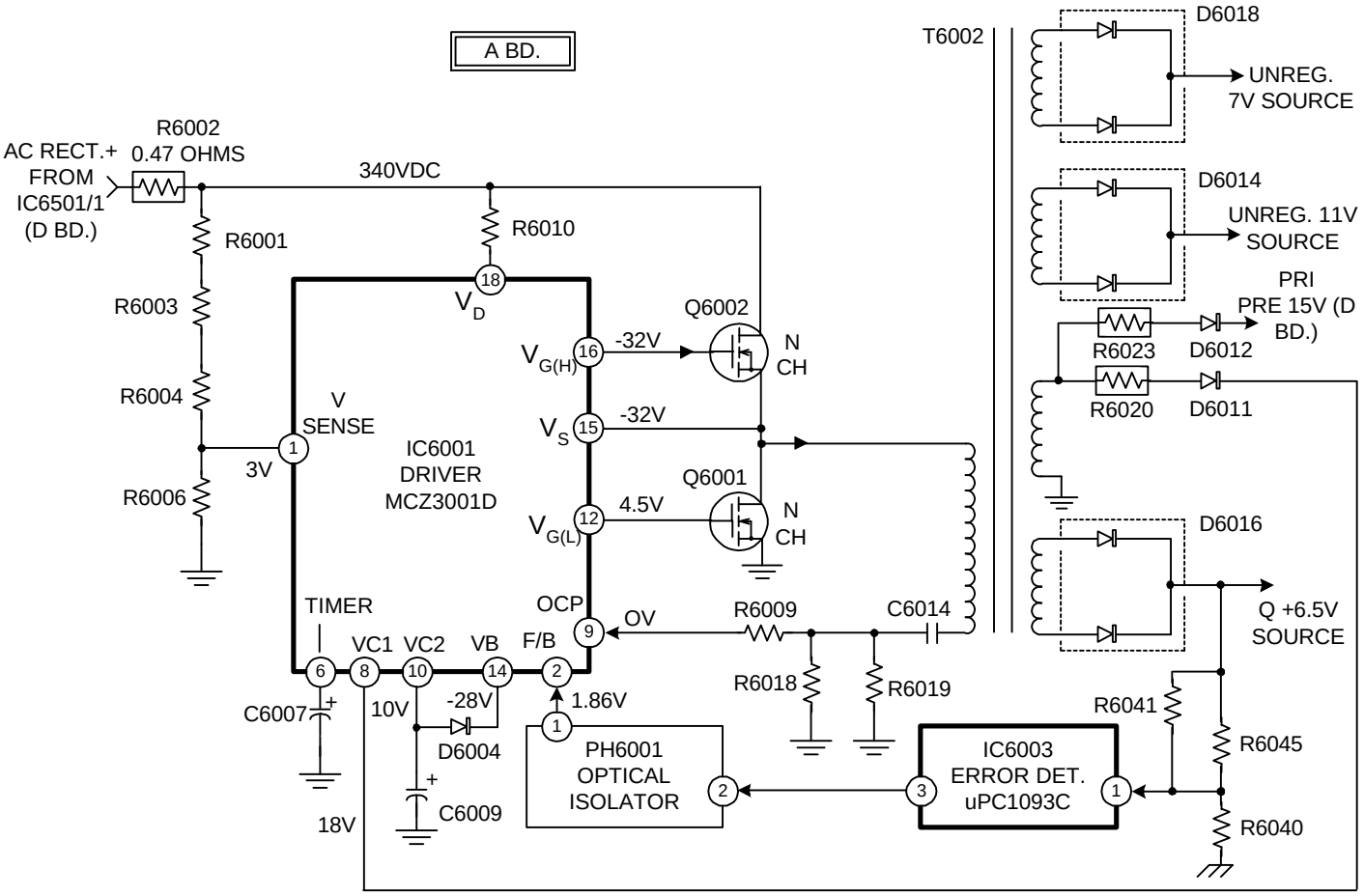


FIGURE 6-1 - PRIMARY POWER SUPPLY - HA-3 CHASSIS 23TVP12 1341 8/30/01

Oscillator Start Up

The oscillator within IC6001 starts if the V Sense input voltage at pin 1 is above 1.3Vdc, but less than 8Vdc. Sample voltage from pin 18 is then used to run the internal oscillator. The initial frequency is approximately 200kHz. The low amplitude initial oscillator signal is output IC6001/pins 12 and 16 into the driver/output stage.

Driver / Output stage

The oscillator voltage output at pins 12 and 16 use drivers Q6001 and Q6002 to develop T6002 secondary voltages. IC6001's oscillator will shut down if the driver transistor's current is excessive. To prevent premature shutdown, the timer capacitor C6007 delays the shutdown.

VC1 Powers IC6001

Although the oscillator is running, at this initial frequency of 200kHz there is insufficient current from T6002 to produce any unregulated 7V or 11V voltage because of the load. On the other hand, there is very little load on D6011 and D6012, so they output about 15V each at the cathodes (normally about 18Vdc).

The voltage from D6011 is returned to IC6001/pin 8 (VC1) to serve as regulated B+ for the IC.

IC6001 Normal Operation

At start up, IC6001 initially uses current limited B+ from pin 18 to power internal drivers. These internal drivers amplify the oscillator signal and get it out to pins 12 and 16. The power for the internal drivers initially come from pin 18, but ultimately comes from pins 10 (VC2) and 14 (VB) when the power supply stage begins working. VC2 provides the voltage for the bottom driver (pin 12) while VB provides the voltage for the top driver (pin 16).

The VC2 voltage comes from the 18Vdc input VC1 (pin 8) that is internally regulated to 10Vdc. The 10Vdc from VC2 is used to make VB voltage at pin 14. Because there is a square wave at pin 14 (internally from pin 15), D6004 and C6009 are necessary to keep the DC voltage at pin 10 and the signal at pin 14 separate. D6004 brings +10V from pin 10 into VB pin 14 to power the top internal driver (pin 16).

The reason VB pin 14 measures –28 is because pin 14 starts at the same voltage as pin 15 (-32Vdc), but +10Vdc is added from D6004. That brings the –32Vdc (+10V =) to -22. Because there is a 50% duty cycle square wave at pin 14, the voltmeter averages the increase so only half of +10V is measured, producing approximately –32 +5V = -28V at VB pin 14.

The result is a VB voltage that is approximately +5V (average) above the reference voltage at IC6001/pin 15. This voltage supplies the top internal driver that amplifies the oscillator signal that leaves IC6001/pin 16.

Secondary Power Supply Starting

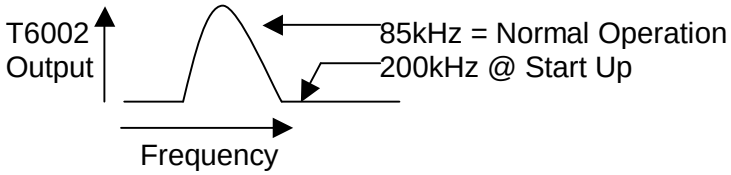
The Pri Pre 15V output of the primary power supply (D6012) is used to enable the secondary power supply. At start up, the primary oscillator frequency is HIGH so low secondary voltages are output. Pri Pre 15V is only 10Vdc at start up but rises to a normal 18Vdc. When it rises to 15.6Vdc, the Secondary Power Supply can start. Therefore, the Secondary Supply cannot start until the Primary Supply is running normally.

Regulator Stage

Concept

By controlling the frequency of the power supply oscillator, T6002's secondary output voltage can be regulated. T6002's secondary output voltages are dependent upon the match between the output resonate circuit (T6002 = L, C6019 = C) and the oscillator frequency. When IC6001's oscillator frequency is the same as the resonate circuit frequency, there is maximum power transferred in T6002, producing maximum output voltage. By setting the oscillator frequency above resonance, T6002's output voltage can be regulated. See Figure 6-2 for the power output of power transformer T6002.

Figure 6-2 – T6002 Output



Output Voltage Control

The regulating stage uses error detector IC6003 and optical isolator PH6001 to monitor the Q+6.5V output from T6002. If the Q+6.5Voutput is LOW, as it is at initial start up (Chart 6-1), the voltage fed back to IC6001/pin 2 goes HIGH, decreasing the oscillator frequency. The decrease in frequency increases the output of the T6002 transformer, until +6.5Vdc is reached.

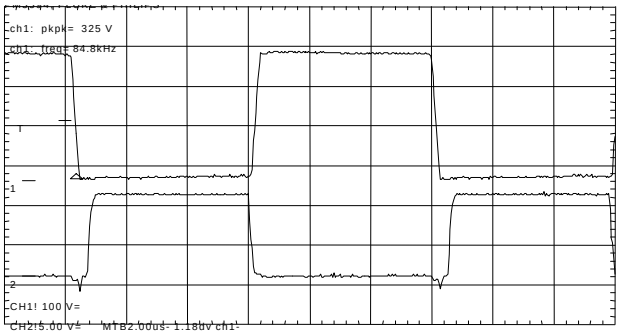
Chart 6-1 - Regulation Stage – Error Correction Voltages

Q+6.5V Output (D6016)	PH6001/pin 2	IC6001/pin 2
Low ⇩	High ⇧	High ⇧

In the following Waveform 6-1, both drive outputs from IC6001/pins 12 and 16 are shown (channels 1 and 2). The outputs are complementary, the duty cycle is 50% and the frequency has dropped down from 200kHz to 85kHz during normal operation. When the top Driver (Q6002) is ON, the bottom Driver (Q6001) is OFF.

Ch 1

Ch 2



Waveform 6-1 - Primary PS Oscillator - Normal operation - 85kHz			
Channel	Name	Location	Voltage
1	Top Driver Output	Q6002/gate	340Vp-p
2	Bottom Driver Out	Q6001/gate	12Vp-p (4.6Vdc)
Time base = 2usec/div.			

Testing

Chart 6-2 shows what is necessary to start and run the primary power supply and Chart 6-3 lists the voltages of the power supply's IC6001.

Chart 6-2 - Checks for Primary power supply operation		
Check Point	Normal	Description
1. R6006 (Fusible)	340Vdc	P.S. Input voltage
2. CN6005/ pin 5	>+15.6Vdc	Pri-Pre 15V. Checks P.S. Output
3. IC6001/ pin 2 (Feedback voltage)	1.9Vdc	Feedback Voltage. Troubleshooting - If step 2 voltage is low, measure IC6001/pin 2. If pin 2 is High (4V) - problem is around IC6001. If pin 2 is Low (0-1V), problem is the feedback path IC6003, PH6001.
4. IC6001 voltages. See chart 6-3.		

Chart 6-3 - IC6001 Voltages (Power ON, Video 1 input, Dark screen)								
1.	**2.**	**3.**	**4.**	**5.**	**6.**	**7.**	**8.**	**9.**
3.0V	1.8V	2.2V	2.5V	0V	0V	4.5V	18.4V	0V
10.	**11.**	**12.**	**13.**	**14.**	**15.**	**16.**	**17.**	**18.**
10V	0V	4.5V	-0.2V	-28V	-32V	-32V	-0.3V	313V

Hot ground is at CN6501/pin 6 (black wire).

Chart 6-4 - IC6001 (MCZ3001D) Pin Description			
Pin - Name	Description	Pin - Name	Description
1 - Sense	ON/OFF input for the IC. IC ON = 1.5-7Vdc.	8 – VC1	Power for IC. Input voltage limits = 15.6V – 33V
2 – F/B	Feedback control voltage for regulation. Needs bias current feed of 80uA min. Open circuit triggers IC shutdown.	9 - OCP	When input voltage reaches 0.2Vdc, the IC momentarily enters high freq, low voltage output. Max = 5Vdc
3 - Ct	Determines Oscillator minimum freq	10 – VC2	10.5dc Output (regulated from VC1) & low driver (pin 12) pwr.
4 – Rt	Determines Oscillator minimum freq	14 - VB	10.5dc Input for high driver (pin 16).
6 - Timer	External cap sets delay time to enter high freq, low voltage output (protect state). After four entry's, the osc stops but can be reset by removing Vcc (pin 8) voltage.	15 - VS	Reference for high side driver.
7 - SS	External cap determines initial start freq. (200kHz in this TV).	18 - VD	Start up voltage for VC1, low & high drivers internal to the IC. Max = 600V/12ma

Protection

See Chart 6-5 below. IC6001 stops operating and enters a protective stage when:

Chart 6-5 - IC6001 enters a protective state			
Protection Cause	Location	Normal	Trip
1. Input V Sense input voltage too high	IC6001/pin 1	3V	8.3V
2. Primary PS Output too high	IC6001/pin 8 (VC1)	15Vdc	33Vdc
3. No regulation feedback (error voltage) *	IC6001/pin 2	1.86Vdc	0V (open)
4. Excessive Driver current(Q6001,2)	IC6001/pin 9	0Vdc	±0.2Vdc
5. IC temperature	Diode Internal to IC6001	?	155 C
* IC Output does not stop. Oscillator output changes from continuous normal operation to output bursts			

RESET IC6001 = Unplug the AC line cord, (or shut off the TV if you can determine that) and wait 10 seconds.

Secondary Power Supply (HA-3 & RA-5A Chassis)

The Primary and Secondary power supplies are similar in operation and circuitry using the same IC and driver/ output stage. They differ in schematic nomenclature and output voltages. The HA-3 simplified secondary power supply shown in diagram 24 contains the RA-5A chassis nomenclature in parentheses.

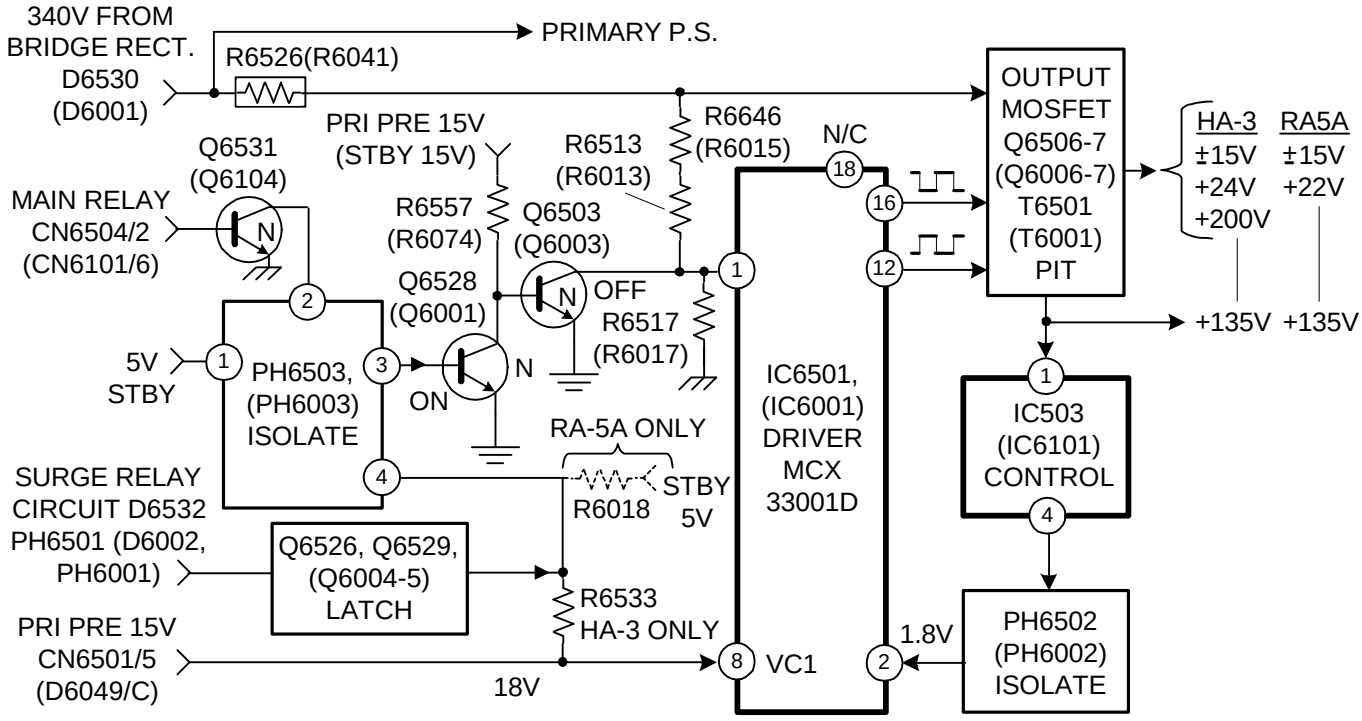


FIGURE 7-1 - SECONDARY P.S. HA-3 (RA-5A) CHASSIS 24TVP12 1371 8/30/01

Start UP

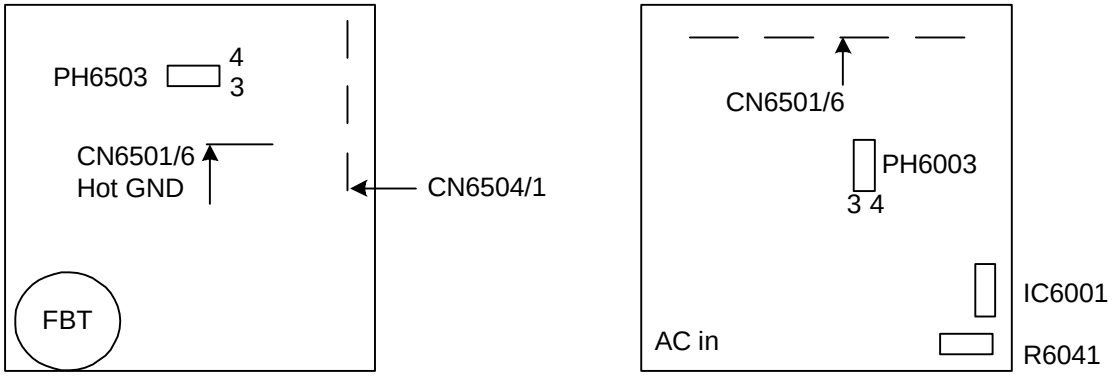
Although IC6501 is identical to IC6001 found in the Primary power supply, IC6501/pin 18 in this supply is not connected to 340Vdc. This means the VC1 voltage at pin 8 must be input externally to this stage to start IC6501's oscillator (during or after V sense at pin 1 senses voltage). Refer to Figure 7-1 as you follow the following Secondary Power Supply start up sequence:

1. 340Vdc (B+) is applied to this stage from bridge rectifier D6530.
2. Pri Pre 15V voltage from the Primary power supply is applied to IC6501/pin 8. It must be at least 15.6Vdc to enable IC6501's internal oscillator.
3. Main Relay signal from Main Micro IC001/pin 72 (HIGH at CN6501/pin 5) turns ON Q6531, PH6503 and Q6528. Q6528 turns OFF Q6503, enabling voltage to appear at IC6504/pin 2.
4. Voltage divider R6646, R6513, and R6517 deliver at least 1.3Vdc to IC6501/pin 1.
5. IC6501 turns ON using voltage from pin 8 to run the oscillator.
6. An internal diode connected between pin 8 and 10 supplies voltage to VC2.
7. Oscillator signal outputs IC6501/pins 12 and 16.

Testing for NO Start

If the secondary power supply does not start, use Chart 7-1 to determine if an input to the D or G board is missing: Refer to Figure 7-2 for the checkpoint locations on the boards.

Chart 7-1 - Items Needed to Start the Secondary Power Supply				
Item	Checkpoint (use Hot Gnd except noted)		From	Purpose
	HA-3 Direct View	RA-5A PJ TV		
340Vdc (B+)	D board CN6501/pin 1 / Fusible R6526	G board Fusible R6041	Bridge Rectifier D6530	Powers the Driver/Output
Pri Pre 15V voltage	D board CN6501/pin 5	G board IC6001/pin 8	Primary Power Supply secondary – Pri Pre	Starts the oscillator when more than 15.6Vdc.
Main Relay voltage	D board CN6504/pin 2 = 4.9Vdc (cold Gnd)	G board CN6101/pin 6 = 5V (cold Gnd)	Main Micro IC001 (B board)	Enables Sec PS Osc IC6501 when HIGH
Surge Relay	D board PH6503/pin 4 = 6.3Vdc	G board PH6003/pin 4 = 4.5Vdc	Primary Power Supply secondary -Sub 7V or Sub 6.5V	Stop the secondary PS if the Surge Relay does not close after power ON.



HA-3 Chassis - D Board

Figure 7-2 Checkpoint Locations

RA-5A Chassis - G Board

Regulation

The +135V line to the Horizontal Output stage is fed back to IC6501 for regulation of the secondary power supply. Error Control IC6503 and Optical Isolator PH6502 control regulation. If the +135V output rises, the voltage at IC6501/pin 2 lowers to correct. A reduced voltage increases the oscillator frequency and decreases the output voltages of T6501.

Testing for Low B+ or Shutdown

The typical error correction feedback voltage at IC6501/pin 2 is 2Vdc. By verifying the +135V B+ at R6598 and measuring the feedback at IC6501/pin 2, you can determine if the problem is in the basic oscillator stage or in the error regulator stage. See Chart 7-2, Chart 7-3 and Chart 7-4 on the following page:

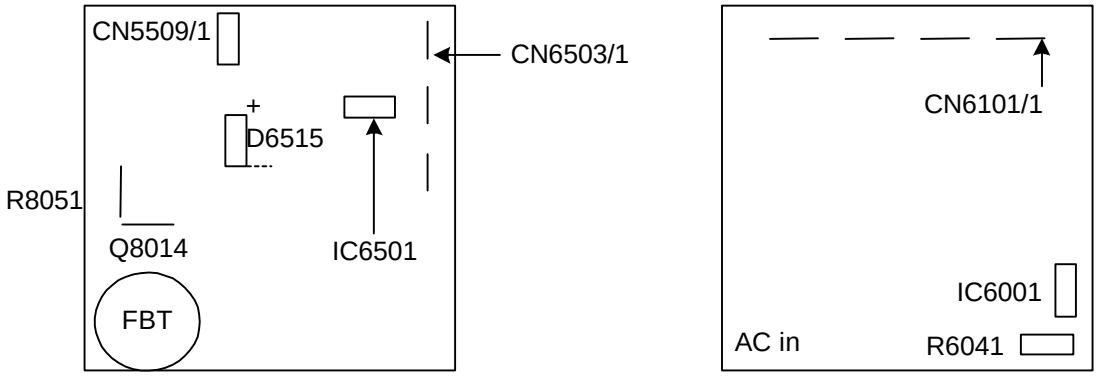
Chart 7-2 - Follow procedure 1-3 to locate PS Shutdown problem		
1. Measure B+ at R6598 (0.27 ohms fusible at 1W)	**2. Measure IC6501/pin 2 Voltage**	**3. Problem area**
B+ is LOW or 0V	Higher than 2V	Oscillator stage IC6501
	Lower than 2Vdc	Error regulating stage IC6503/PH6502
B+ is HIGH (shutdown – Stby light blinks 3 times)	Higher than 2V	Error regulating stage IC6503/PH6502
	Lower than 2Vdc	Oscillator/Driver Stage IC6501

Chart 7-3 - IC6501 Typical Voltages (Power ON, Video 1 input, Dark screen)								
1.	**2.**	**3.**	**4.**	**5.**	**6.**	**7.**	**8.**	**9.**
2.5V	1.8V	2.2V	2.5V	0V	0V	4.0V	18.3V	0V
10.	**11.**	**12.**	**13.**	**14.**	**15.**	**16.**	**17.**	**18.**
10V	0V	4.7V	0 V	-15V	-19V	-19V	0V	1.5V

Use the Hot ground shown in figure 1 at CN6501/pin 6 (black wire).

Chart 7-4 - Checking the Primary PS Output			
HA-3 Chassis		RA-5A Chassis	
Voltage	Checkpoint	Voltage	Checkpoint
±15V	15V Bridge Rectifier D6514	±15V	CN6106/pins 7 & 9
+24V	CN6503/pin 7 or 8	±22V	CN6106/pins 4 & 6
+135V	CN5509/pin 9	+135V	CN6106/pin 1
+200V	Fusible R8051 or Q8014/D		

Use Cold Ground such as the tuner or FBT shield. Heat sinks are not reliable ground points.



HA-3 Chassis - D Board

RA-5A Chassis - G Board

Figure 7-3
Voltage Checkpoint Locations

Protection Block (HA-3 Chassis)

Refer to Figure 8-1 for the following overview of the protection circuits. When a failure occurs, this TV will protect the remainder of its circuitry in one of the following ways:

- TV shutdown (AC relay is turned off);
- TV Latched OFF (AC relay is held off); or
- A dark picture (no RGB signal to the CRT cathodes).

When Main Micro IC001 places the TV in a protective state, IC001 also indicates the cause by blinking the Standby LED a number of times, pauses, and then repeats the same count.

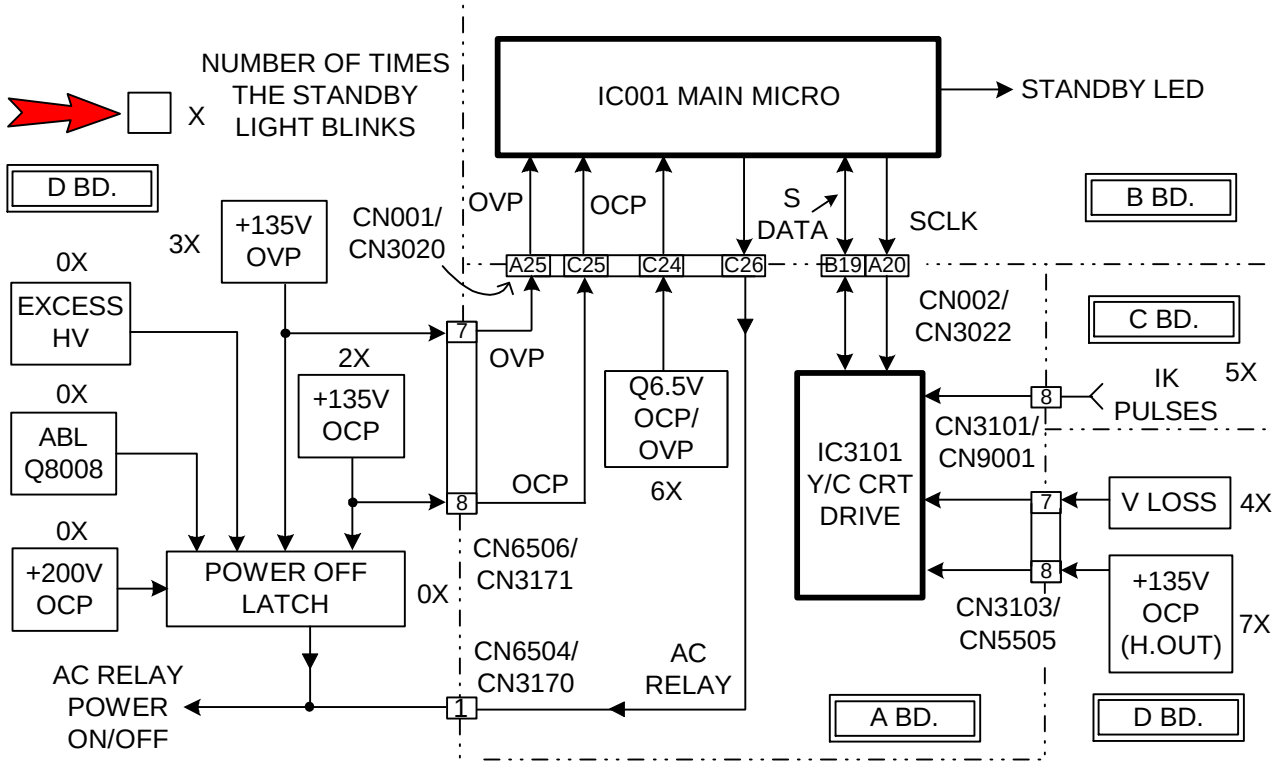


FIGURE 8-1 - PROTECTION BLOCK 20TVP12 1338 9/4/01

There are seven protected areas summarized in Chart 8-1**.** Chart 1 also lists the signal that triggered the protection. If no signal triggered the protection, suspect Micro IC001 on the B board and the latch transistors (Q6522/ Q6530) on the D board of causing the TV shutdown. Figure 8-2 shows the location of Chart 8-1's protection signal checkpoints.

Chart 8-1 - Shutdown Causes				
Stby LED Blinks	Protected areas	Bd	Check Point	Normal Ck Pt voltage
0 X	+200V OCP (HV) / Over HV	D	Q8009/C	0.1Vdc
2 X	+135V OCP	D	CN6506/ pin 8	0V
3 X	+135V OVP	D	CN6506/ pin 7	0.1V
4 X	V Out Loss	D	CN5505/ pin 7	0.78V
5 X (pix blanked - TV remains ON)	IK balance	C/A /G2 adj	C Bd – CN9001/ pin 8	3 pulses in vertical interval.
6X	Q6.5V OVP & OCP	A	D6021/ cathode	0Vdc
7X	H Out OCP	D	CN5505/ pin 8	0V

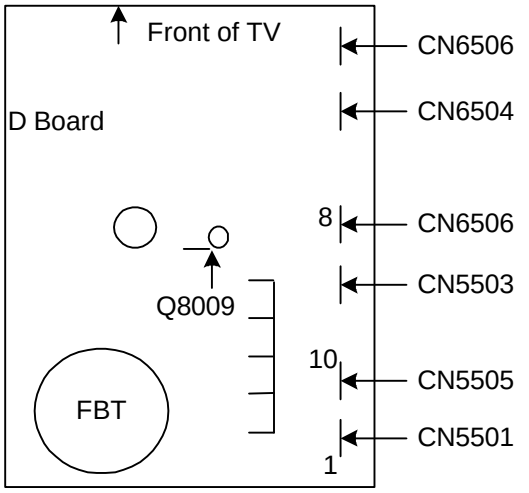


Figure 8-2

Pin 1 of each connector begins at this end

Protection Circuits

After the TV enters a protective state, the standby light blinks to identify one of seven problem sections. Each section consists of not only the protected circuit (load) but also the sensing circuit that monitors the fault. A description these seven sections consist of the sensing circuit itself so you know how the load is being protected and a test for the load.

Standby light blinks 0 times – TV Shutdown

Refer to Figure 8-3 for the circuit description and Flow Charts A and B (Figures 8-4 and 8-5) for the testing procedure.

Circuit – When the TV shuts down and the Standby light will not indicate the trouble area, five circuits are suspect:

- 200V OCP (HV Over current protection)
- ABL voltage too LOW (Video Output Failure)
- Excessive HV
- Surge Relay did not energize
- Shutdown Latch Circuit failure

1. 200V OCP - R8043 and Q8009 monitor the current on the +200 volt line. This 200-volt line supplies the High Voltage Converter stage, which feeds the flyback transformer. The flyback generates HV, focus voltage and ABL voltage. A short in the flyback or excessive high voltage will demand sufficient current to shut down the TV. When the voltage across R8043 reaches 1.2Vdc, Q8009 outputs a HIGH that passes through D8003 to trigger the latch formed by Q6530/Q6532. The latch grounds the voltage required to sustain relay driver Q6527 and the TV shuts off. Since there is no connection to the Main Micro IC001, the standby LED will not indicate this failure.

2. ABL voltage - The ABL voltage from the flyback T8001 at pin 1 is monitored by IC8001. As the CRT draws more current from the flyback's HV output, the ABL voltage reduces. If this voltage drops to 0Vdc, IC8001 outputs a HIGH for as long as the TV is powered ON. The HIGH passes through D8027 to trigger the Q6530/Q6532 latch that finally shuts off the TV set.

3. Excessive HV - To shut down the TV when there is excessive HV, a winding of the FBT produces a voltage proportional to the HV. This secondary AC voltage is rectified by D8014 and applied to protection latch IC8001.

When D8014's voltage reaches a critical level, IC8001 outputs a HIGH for as long as the TV is powered ON. The HIGH passes through D8027 to trigger the Q6530/Q6532 latch that finally shuts off the TV set.

4. Surge Relay - If the secondary power supply (IC6501) came on but shut down in six seconds, it would seem as though the TV's AC relay had shut off the TV except that the AC relay remains energized.

This unlikely problem could happen if the primary power supply (IC6001 – A board) did not produce the 7Vdc output used to energize the surge relay RY6502 or its contacts did not short out R6516. If the surge relay did not energize after the TV was turned ON, C6595 would continue to charge. When this voltage reaches 0.6Vdc, latch Q6526 and Q6529 would turn ON. This grounds the V sense voltage input to IC6501/pin 1, shutting down the secondary power supply.

5. Shutdown Latch – Finally, an unstable standby voltage or a defect in the basic latch circuit (Q6530 and Q6532) will also cause the TV to shut down without the standby light blinking. This last problem is rare.

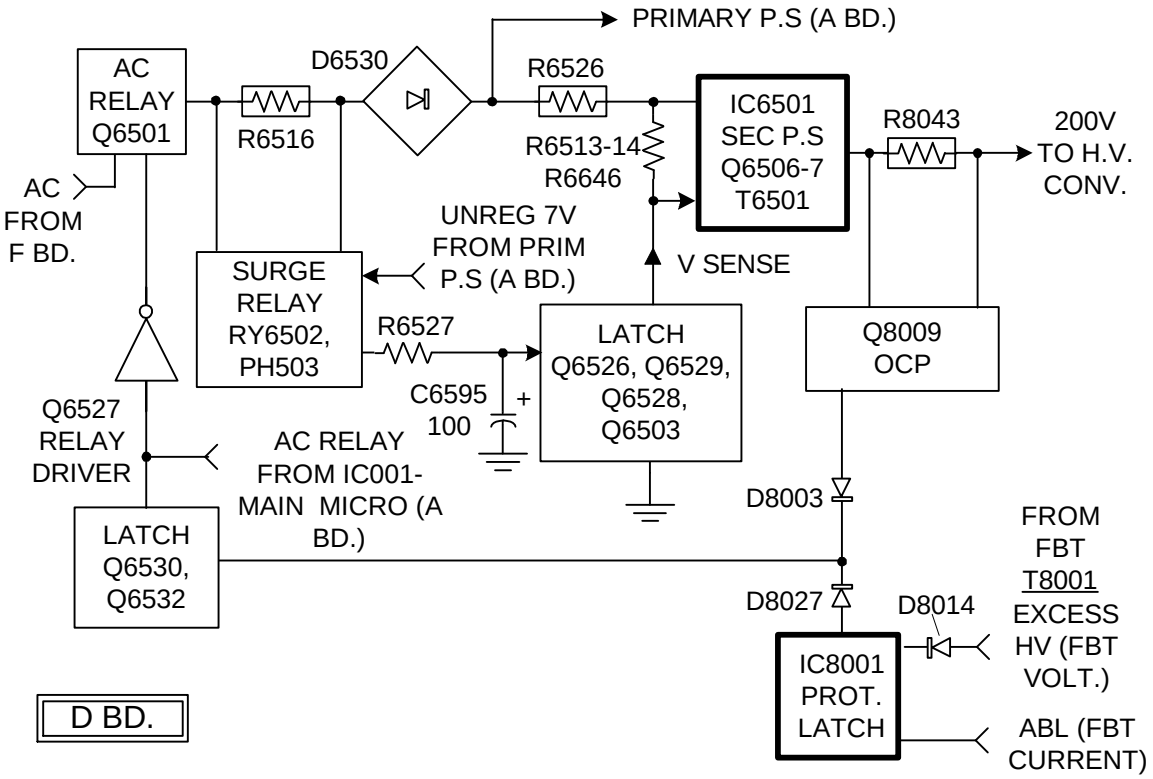


FIGURE 8-3 - SHUTDOWN - NO INDICATION 15TVP12 1333 9/4/01

Testing – If the TV relays turn ON but quickly turn back off with no standby light indication, use these flow charts to determine which one of the five circuits is causing the shutdown:

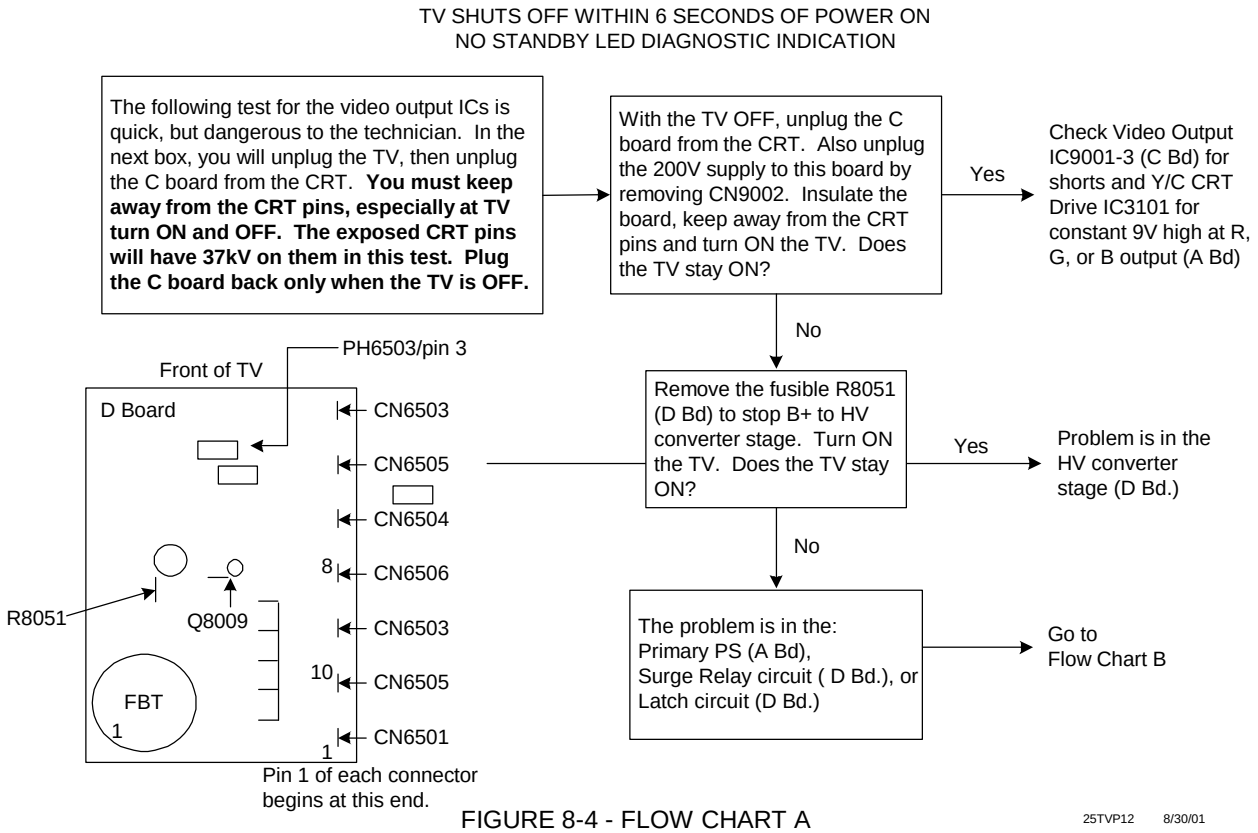

TV SHUTS OFF WITHIN 6 SECONDS OF POWER ON
NO STANDBY LED DIAGNOSTIC INDICATION
The following test for the video output ICs is quick, but dangerous to the technician. In the next box, you will unplug the TV, then unplug the C board from the CRT. You must keep away from the CRT pins, especially at TV turn ON and OFF. The exposed CRT pins will have 37kV on them in this test. Plug the C board back only when the TV is OFF.
With the TV OFF, unplug the C board from the CRT. Also unplug the 200V supply to this board by removing CN9002. Insulate the board, keep away from the CRT pins and turn ON the TV. Does the TV stay ON?
Yes
Check Video Output IC9001-3 (C Bd) for shorts and Y/C CRT Drive IC3101 for constant 9V high at R, G, or B output (A Bd)
No
Remove the fusible R8051 (D Bd) to stop B+ to HV converter stage. Turn ON the TV. Does the TV stay ON?
Yes
Problem is in the HV converter stage (D Bd.)
No
The problem is in the: Primary PS (A Bd), Surge Relay circuit (D Bd.), or Latch circuit (D Bd.)
Go to Flow Chart B
Front of TV
PH6503/pin 3
D Board
CN6503
CN6505
CN6504
CN6506
CN6503
CN6505
CN6501
R8051
Q8009
FBT
8
10
1
1
Pin 1 of each connector begins at this end.

FIGURE 8-4 - FLOW CHART A 25TVP12 8/30/01

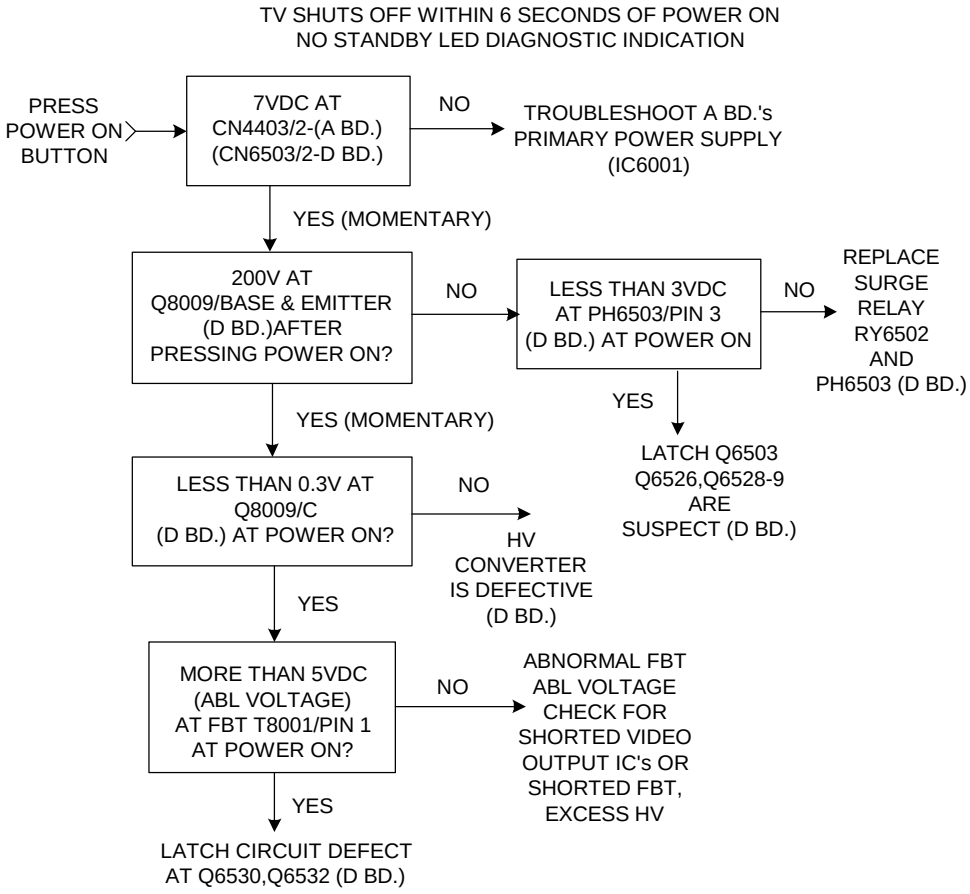

TV SHUTS OFF WITHIN 6 SECONDS OF POWER ON
NO STANDBY LED DIAGNOSTIC INDICATION
PRESS POWER ON BUTTON
7VDC AT CN4403/2-(A BD.) (CN6503/2-D BD.)
NO
TROUBLESHOOT A BD.'s PRIMARY POWER SUPPLY (IC6001)
YES (MOMENTARY)
200V AT Q8009/BASE & EMITTER (D BD.)AFTER PRESSING POWER ON?
NO
LESS THAN 3VDC AT PH6503/PIN 3 (D BD.) AT POWER ON
NO
REPLACE SURGE RELAY RY6502 AND PH6503 (D BD.)
YES
YES (MOMENTARY)
LATCH Q6503 Q6526,Q6528-9 ARE SUSPECT (D BD.)
LESS THAN 0.3V AT Q8009/C (D BD.) AT POWER ON?
NO
HV CONVERTER IS DEFECTIVE (D BD.)
YES
MORE THAN 5VDC (ABL VOLTAGE) AT FBT T8001/PIN 1 AT POWER ON?
NO
ABNORMAL FBT ABL VOLTAGE CHECK FOR SHORTED VIDEO OUTPUT IC's OR SHORTED FBT, EXCESS HV
YES
LATCH CIRCUIT DEFECT AT Q6530,Q6532 (D BD.)

FIGURE 8-5 - FLOW CHART B 22TVP12 1340 9/4/01

Standby light blinks two times – TV Shutdown

There are two +135V OCP monitoring circuits. The first circuit will cause the Standby light to blink two times and the second will cause the light to blink seven times. Both sensing and output circuits are on the D board but the indicating circuit is on the B board.

Circuit - Refer to Figure 8-6 for the following circuit and testing procedure. The sensing circuit consists of R6598, R6591, Q6520, Q6521 and Q6524. It monitors the current on the +135V line from the Secondary Power Supply. The +135 volt line supply the following loads:

- Velocity modulation (V) board
- Horiz Output (Q5030) and PWM (Q5003) stage (D board)
- The HOT supplies +200V to the RGB Output ICs (C board).

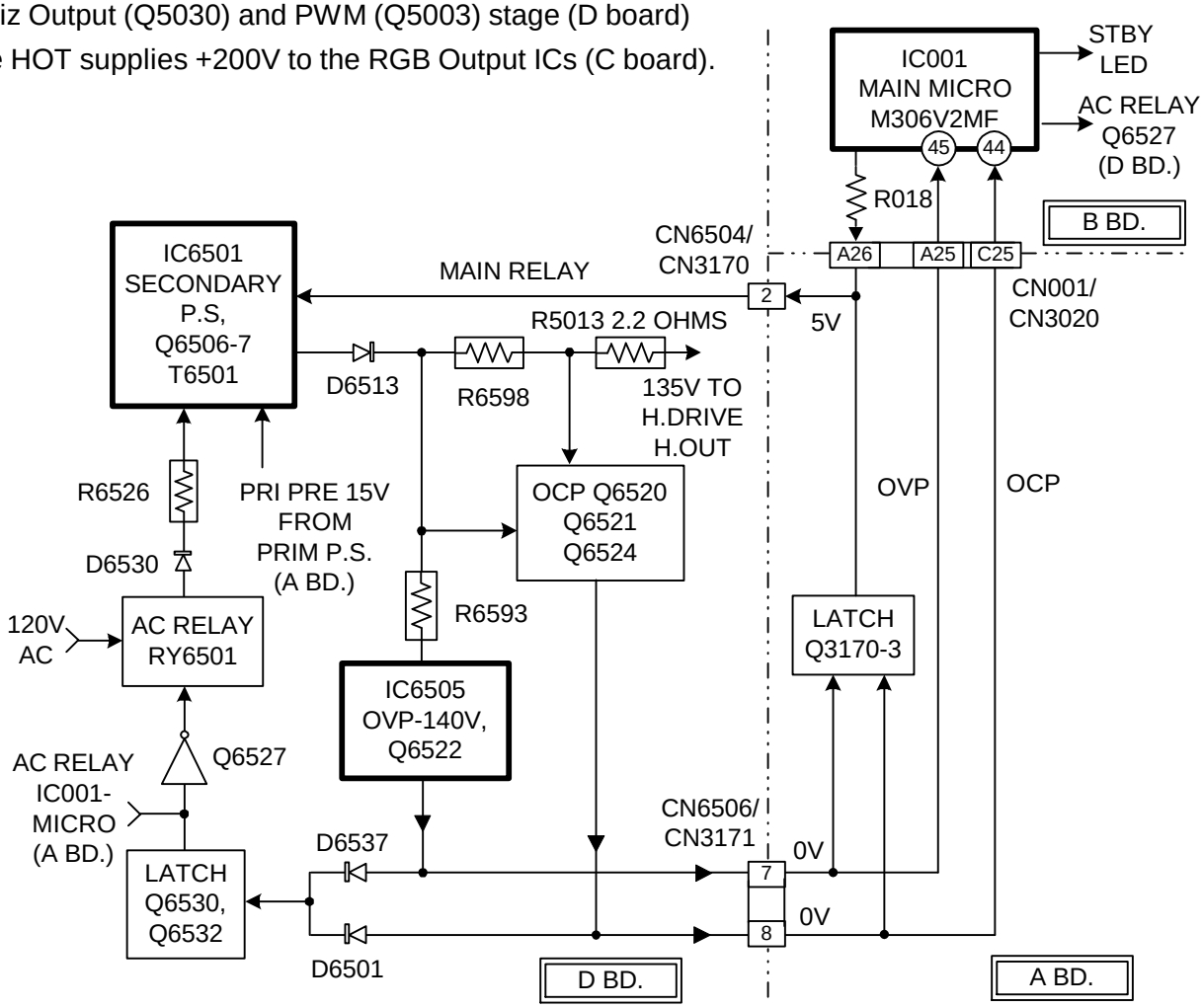


FIGURE 8-6 - SHUTDOWN - 2X, 3X, INDICATION 16TVP12 1334 9/4/01

Testing – You can test the sensing circuit by removing R5013 (disconnects the load) and power up the TV to see if the standby LED blinks 2X. Since the sensing circuit has a low failure rate, the TV will usually stop the 2X blinking, indicating the load is at fault. The +135Vdc load goes to the H. Output/PWM stage on the same D board and the velocity modulation coils on the V board.

To locate the problem, monitor CN6506/pin 8 as you power ON. The normal voltage here is 0Vdc. If the voltage reaches 1.2V, disconnect the V board and try again. If the CN6506/pin 8 voltage still rises to 1.2V, test the H Driver transistor Q5028, H Output transistor Q5030 and PWM transistors (Q5003, Q5011) or replace the entire D board.

The circuit description and simplified schematic of this PWM-H Output section is in the DTV-02 training manual on page 37.

Standby light blinks three times – TV Shutdown

Circuit – Referring to Figure 8-6, the maximum voltage the +135V line can rise to from the D board is +140V before the TV is shut down. IC6505 and Q6522 sense the danger and apply a voltage through D6537 when this limit is reached. This voltage triggers latch Q6530/Q6532 that shuts off the TV (RY6501 = OFF).

Testing - To verify the trip condition, on the D board, monitor CN6506/pin 7. If this voltage rises above 0.6Vdc, the problem is on the D board, either in the sensing circuit (IC6505/Q6522) or the secondary power supply (IC6501).

To determine if the problem is in the sensing circuit or the secondary power supply you will need a peak reading DVM. Monitor the +135Vdc at CN5509/pin 9 (D Bd). Note the reading at power ON. If this voltage is too high, go to the regulating circuit that is found in the Secondary Power Supply chapter of this book. Suspect the Control IC6503 and perhaps static/lightning damage to PH6502. If the voltage peaks at a normal 135Vdc, the problem is in the IC6505/Q6522 sensing circuit.

Standby light blinks four times – TV Shutdown

Refer to Figure 8-7 for this circuit and testing.

Circuit - A vertical failure because of the output IC or secondary power supply (both on the D board) will cause the Y/C Jungle, CRT Drive IC3101 (A board) to send emergency serial data to Main Micro IC001 (B board). IC001 turns the TV OFF by dropping the AC relay drive voltage (IC001/pin 69 goes LOW).

Testing - At power on verify +15v and -15V to the vertical output, IC5004/pins 2 and 4, before you suspect the vertical IC5004 itself or discontinuity in the vertical deflection yoke path (plug/socket).

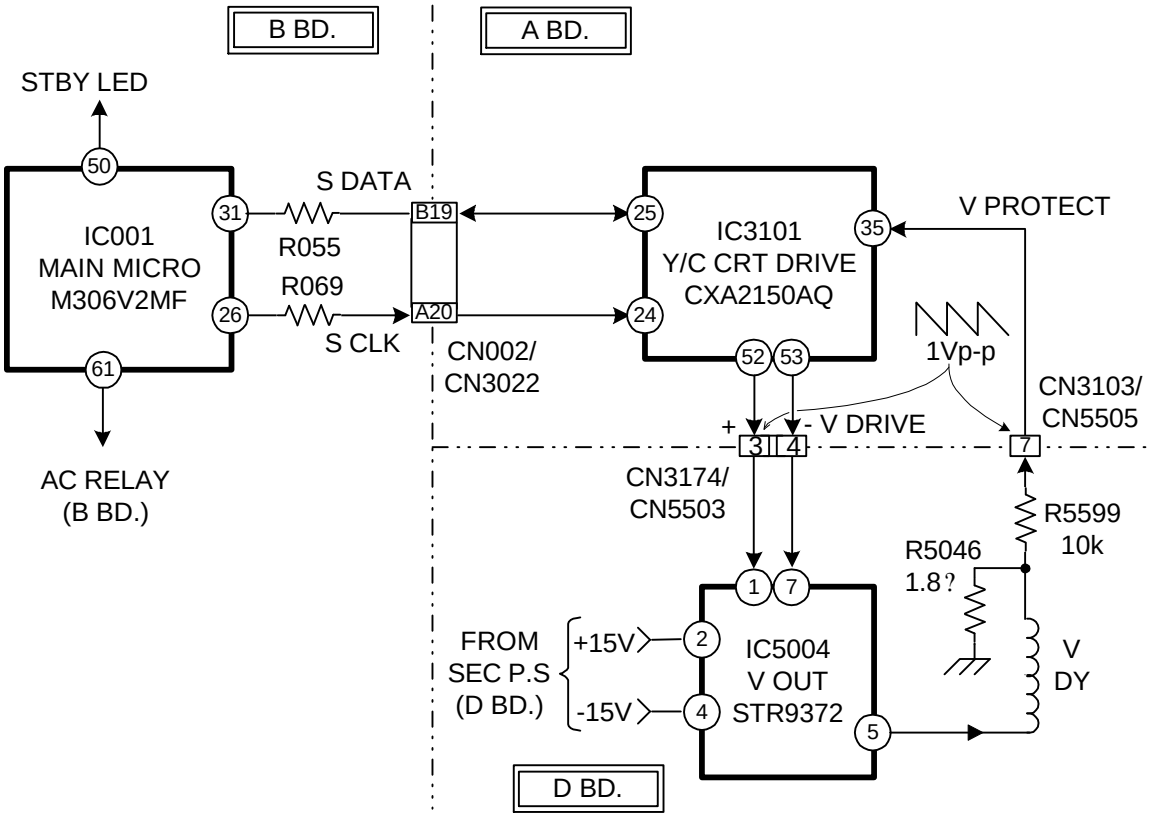


FIGURE 7-7 - SHUTDOWN - 4X INDICATION 17TVP12 1335 9/6/01

Standby light blinks five times – Picture Blanked (dark), sound OK.

Refer to Figure 8-8 for this circuit and testing.

Circuit - Three IK pulses are measured by Y/C, CRT Drive as they return to IC201/pin 58. Each pulse corresponds to the efficiency of each CRT cathode and is used to adjust the RGB gain within IC3101 to maintain color balance while the TV is operating (dynamic adjustment). The IK signals originate from IC3101 in as three bright lines in the vertical-blanking interval at lines 19-21. As the picture tube ages, the IK signals may fall below the threshold for automatic balance adjustment causing IC3101 to mute/blank the substandard picture. Although the picture is blanked, the IK pulses still output IC3101 and the three return IK pulses to IC3101/pin 58 are still operational as long as the TV is ON.

Testing - Increase the G2 control on the CRT's C board. If that does not return cathode current to within operating range so the picture appears, examine each filament to see if it is lit.

The next step uses your scope to determine if there is drive signal to each CRT cathode. Begin by looking for a positive pulse at CN9001/pins 1, 3 and 5 as it enters the C board. Next, check for these signals at each CRT cathode (R, G and B). If they are present, examine the composite IK signal at CN9001/pin 8 of the C board. You should see three pulses that change in level as the G2 control is adjusted. One pulse corresponds to one color and they should be within 15% of each other. The normal IK output from the CRT/C board is about 1Vp-p pulses at pin 8. If these three pulses are present at pin 8, the problem is on the A board about IC3101.

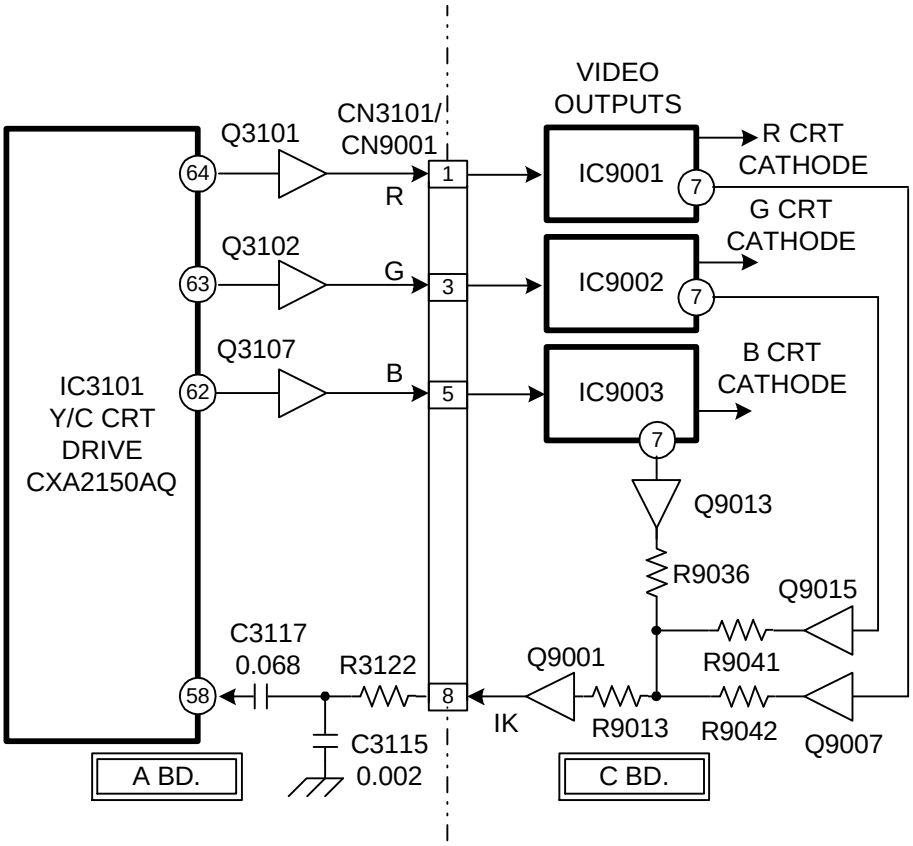


FIGURE 8-8 - BLANKING - 5X INDICATION 19TVP12 1336 9/4/01

Standby light blinks six times – TV Shutdown

Refer to Figure 8-9 for this circuit and testing.

Circuit – IC001/pin 43 monitors the Q6.5Vdc from the Primary power supply (A Bd) to the Q box (QM and QI boards). A short or excessive voltage on the Q6.5Vdc line will cause IC001 to shut off the AC relay (IC001/pin 69 goes LOW).

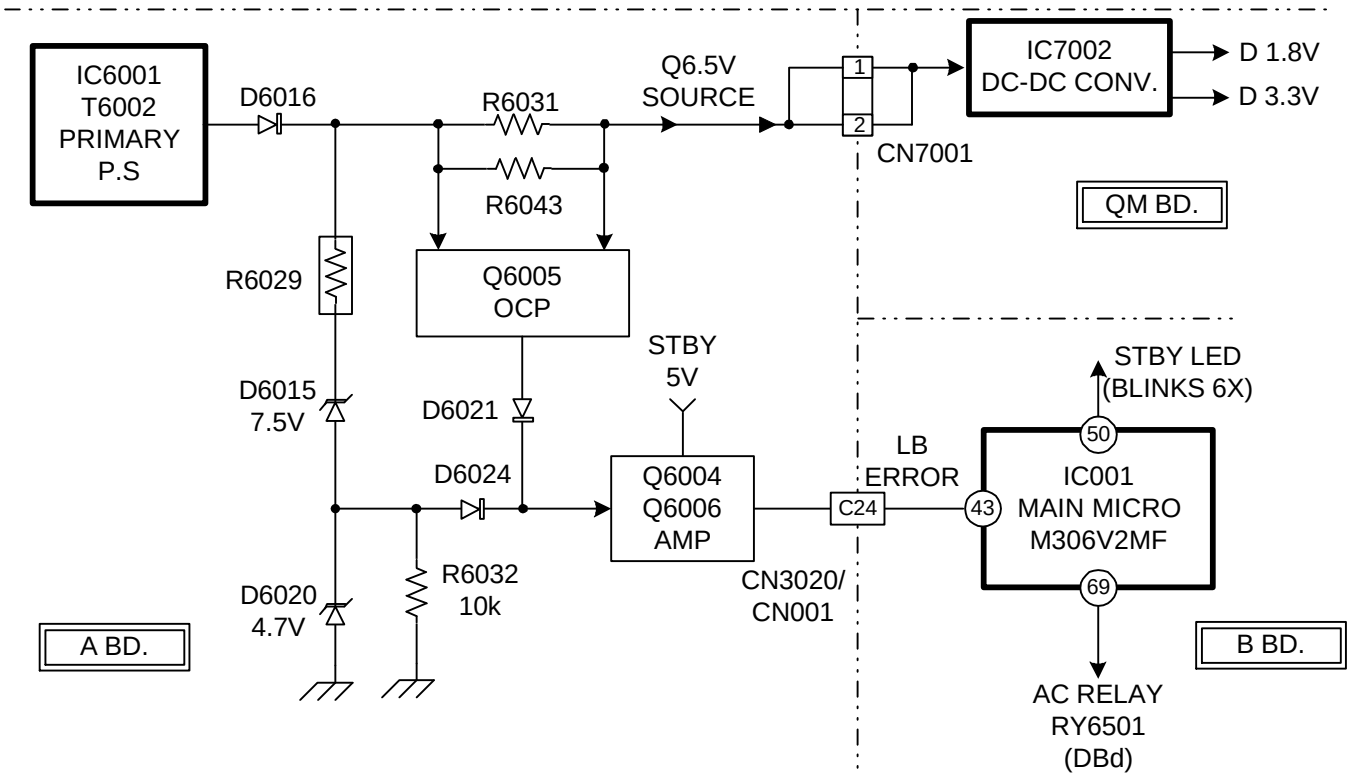


FIGURE 8-9 - SHUTDOWN - 6X INDICATION 14TVP12 1332 8/30/01

Testing – Unplug power to the Q box (CN7001) and power On the TV. If the TV does not shut down, the problem is in the Q box. If the TV still shuts down, the problem is in the primary power supply. Measure "Q6.5Vdc" at CN6005/pins 1 or 2 on the A board at power ON. A high of 8Vdc will trip the protection latch and shut down the TV. The TV will not display A/V without the Q box (dark screen).

Standby light blinks seven times – TV Shutdown

There are two +135V OCP monitoring circuits. The first circuit will cause the Standby light to blink two times and the second will cause the light to blink seven times. Both sensing and output circuits are on the D board, but the indicating circuit is on the B board.

Circuit - Refer to Figure 8-10. The second OCP circuit consists of Q5004, Q5018, and IC5007 on the D board. It monitors the +135V current through R5013 to the PWM Output (Q5003, Q5011) circuitry. This output circuitry supplies B+ voltage (regulated 102Vdc) to the H. Output transistor Q5030. When there is excessive current drawn by the Horizontal Output stage, OCP transistor Q5018 turns OFF, permitting IC3101/pin 34 to rise to a threshold of 1.2Vdc (D board - CN5505/pin 8).

Y/C CRT Drive IC3101 immediately blanks the picture to prevent a CRT line burn and sends instructions (data) to IC001/pin 31 to stop the AC relay voltage, which shuts down the TV.

Normally at power ON, Protect Mute Q3111 on the A board is turned on for five seconds to ground IC3101/pin 34 (CN3103/pin 8). This permits OCP comparator IC5007 (D board) time to stabilize, preventing premature blanking and shutdown at power ON.

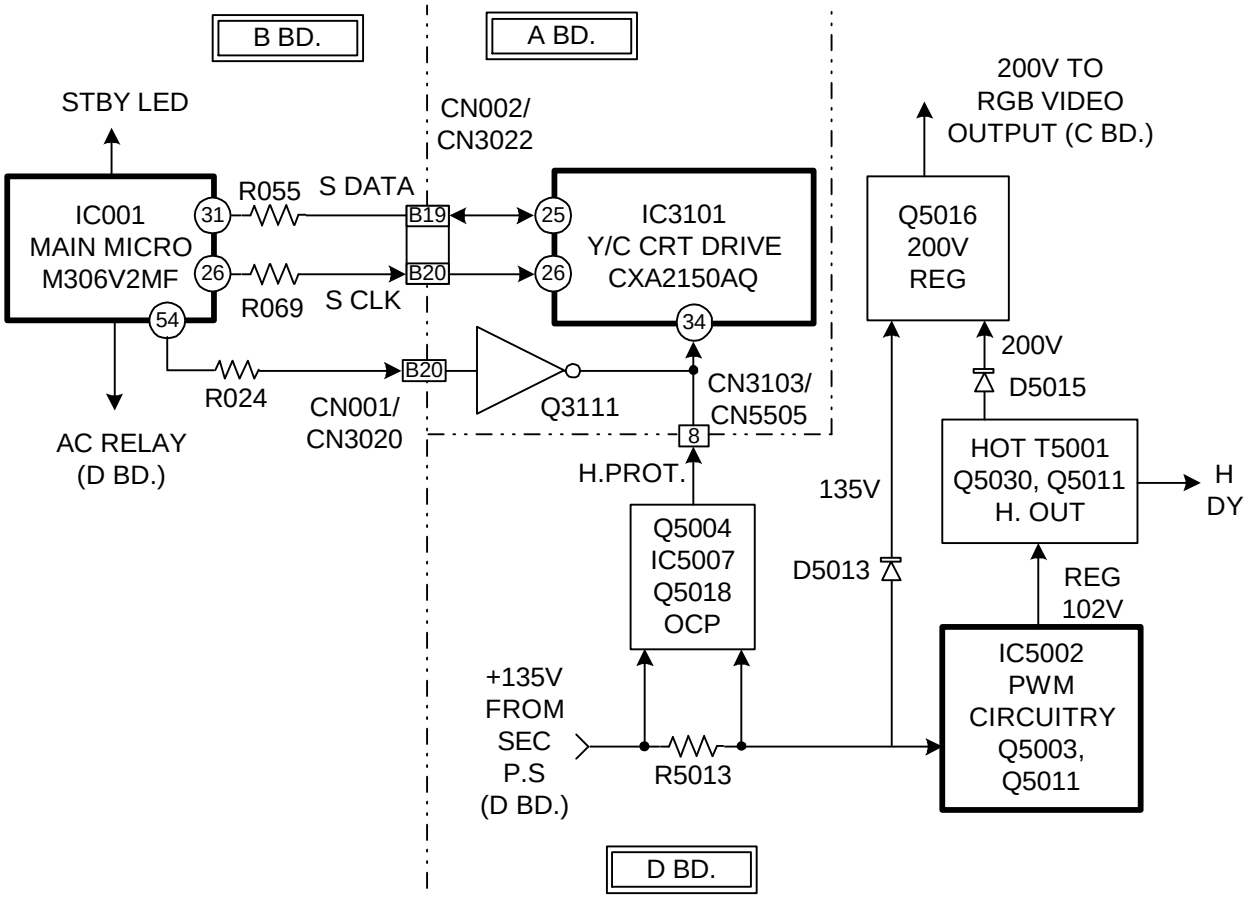


FIGURE 8-10 - SHUTDOWN - 7X INDICATION 18TVP12 1337 9/4/01

Testing - If the Standby light blinks two or seven times, the problem is most likely on the D board where the sensing and Horizontal Output stages are. On the D board, if the Horizontal Output (Q5030), PWM (Q5003/ Q5011) transistors and video output ICs (C board) are good, suspect the components in the sensing circuit (same board). The sensing parts are Q5004, IC5007 and Q5018.

Verify that this circuit is causing the shutdown by disconnecting the H. Output Transistor Q5030 and monitor the voltage at CN5505/pin 8 (D Bd) as you power ON. If this voltage rises above 1 volt, this +135V OCP circuit or Q3111 is responsible. The 135V OCP circuit consists of:

R5013, Q5004, IC5007, delay cap C5006, and Q5018 on the D board (not all parts shown in Figure 8-10).

High Voltage Power Supply

This HV Converter is similar to the two low-voltage power supplies because they both have the same MCZ3001D ICs. This power supply differs only in the start up, voltage output and over voltage (OV) protection. The Flyback Output transformer of this power supply generates regulated 31.5kV and focus voltage for the CRT. Excessive current drawn by this stage will permit Q8009 to shut down the TV set, but there will be no Standby light blink indication. Refer to Figure 9-1 for the overview and Figure 9-2 for the description.

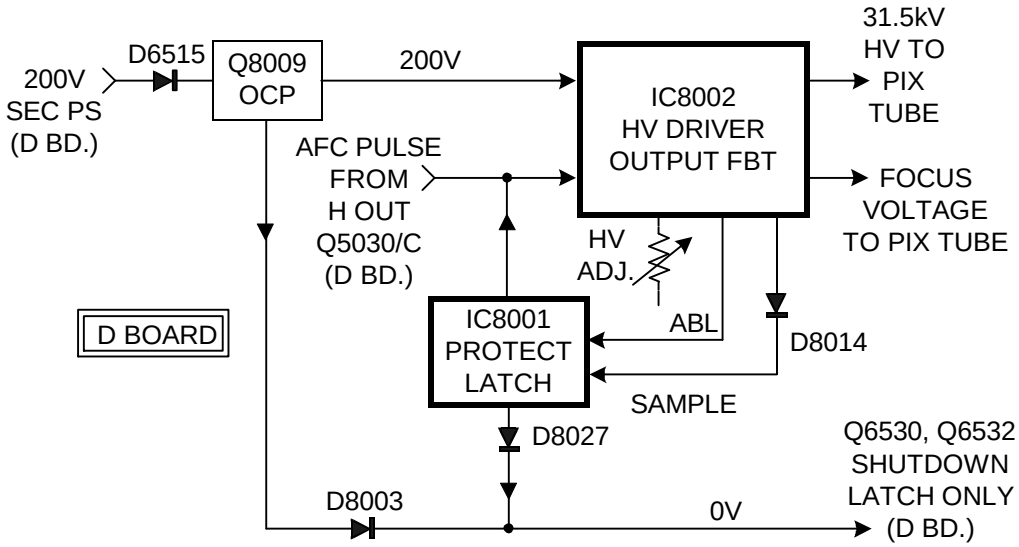


FIGURE 9-1 - HA-3 HV BLOCK 55TVP12 1369 8/30/01

Start UP

Three items listed in Chart 9-1 are necessary to start this HV power supply:

Chart 9-1 - HV Converter Inputs (Starting)		
Name	From	Destination
1. +200V	D6515 & D6517 / cathode(D Bd)	IC8002/18 (199V)
2. +15V	D6514 / cathode (D Bd)	IC8002/8 (14.7V)
3. AFC-PLS	H Out Q5030/C (D Bd) (CN5501/pin 3 = 9Vp-p	IC8002/1 (1.6V)

The Start sequence is as follows:

- The Primary power supply produces low voltages for the Horizontal stage (D board).
- The Secondary power supply produces +135V for the Horizontal stage, along with +200V and +15V for this HV Converter stage.
- The Horizontal Output stage is needed to develop AFC-PLS pulses (CN5501/pin 3 = 9Vp-p) for the HV Converter.
- AFC-PLS pulses turn ON Q8001 and turn OFF Q8002.
- IC8002/pin 1 voltage rises to 1.8V. (1.3Vdc is the minimum to start IC8002).
- IC8002's oscillator starts and drives the flyback transformer.
- The voltage at IC8002/pin 2 decreases from 4V to 2Vdc as the HV climbs to 31.5kV.
- Regulated HV and focus voltage output the flyback transformer.

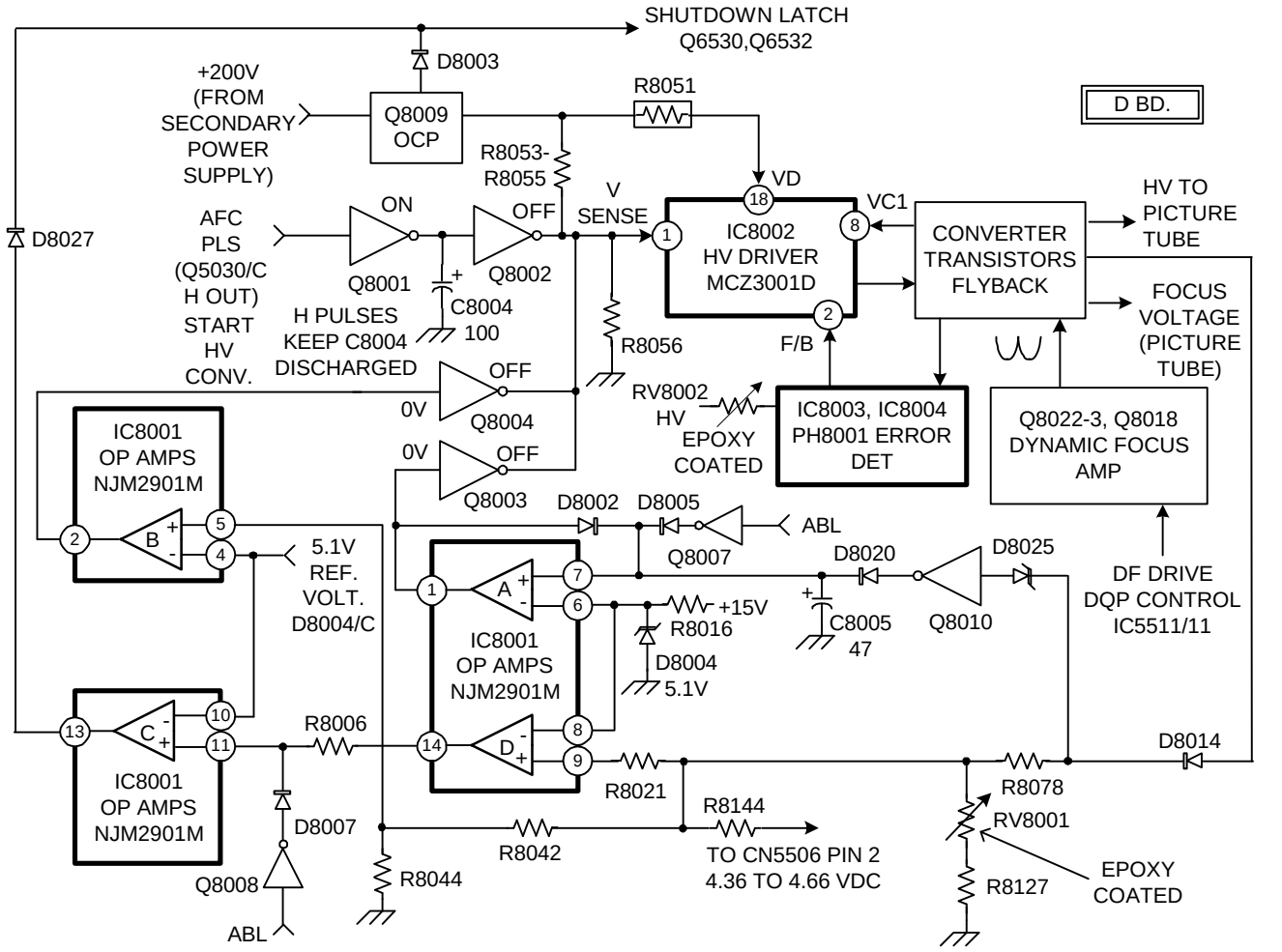


FIGURE 9-2 - HA-3 CONVERTER BLOCK

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Protection

There are two protection circuits for the HV stage. The first causes the HV to stop, leaving the TV's audio to continue operating. The second shuts off the entire TV set.

No or Momentary High Voltage

Excessive HV

A representative sample of this HV is available at the cathode of D8014. Since D8014 is difficult to access, D8025/cathode is the same electrical point but easier to access. D8025/cathode's normal voltage is 32Vdc when the HV is 31.5kV.

This sample voltage from D8014 is applied to IC8001/B to stop the HV if it becomes excessive. IC8001 consists of four op-amps in the same package, all with their negative inputs connected to a +5V reference voltage held by zener D8004.

When the HV is excessive, the sample voltage input IC8001/pin 5 rises higher than the +5V reference voltage, causing IC8001/pin 2's output to go HIGH. The HIGH output is applied to inverter Q8004 that outputs a LOW. This LOW output from Q8004 (collector) grounds IC8002/pin 1 and stops the HV oscillator IC8002.

Below Normal HV

After the TV is turned ON, if the HV drops lower than normal, the HV oscillator will stop. Below normal HV is monitored by IC8001/A. In normal operation, a sample of the HV from D8014 causes 33V zener D8025 to conduct. The HIGH that is output D8014 is turned into a LOW by inverter Q8010. Q8010's LOW output is passed

by IC8001/A to output a LOW that keeps Q8003 turned OFF in normal operation. C8005 keeps IC8001/pin 7 LOW at turn ON when there is no HV, to prevent premature HV shutdown. If the HV drops low for a prolonged period because it is being loaded down or the screen is excessively bright, 33V zener D8025 turns OFF and inverts all the logic states listed above causing the HV to stop.

Excessive Beam Current (ABL)

Excessive current through the flyback transformer will stop the HV if a momentary bright screen (video game, or action movie) caused the current demand. This protection circuit monitors the ABL (ground leg of the picture tube HV feed) line at the FBT using Q8007 and D8005. If the screen brightness rises to a critical level, the low going ABL voltage is inverted by Q8007, causing a HIGH to pass through D8005 into latch IC8001/pin 7. The latch outputs and holds the HIGH at pin 7 that turns ON Q8003. Q8003 in turn grounds V Sense IC8002/pin 1 to stop the HV oscillator. Latch IC8001 resets when the TV is turned OFF.

TV Shutdown

Excessive HV

If the HV rises very fast (faster than the IC8001/B HV kill circuit can respond), IC8001/C and D will shut down the entire TV set. The Standby LED indicator lamp (part of the self-diagnostic circuit) will NOT blink when HV shutdown occurs.

During a defect when the sample HV from D8014 continues to rise, IC8001/D voltage at pin 9 reaches the +5V threshold. The HIGH that is output pin 14 passes IC8001/C to produce a HIGH at pin 13. This final HIGH passes D8027 and is applied directly to the shutdown latch formed by Q6530 and Q6532. When this latch activates, shutdown occurs so fast that it seems the TV set did not turn on at all. An easy way to prove this HV protection circuit caused shutdown is to look for a momentary increase in voltage at D8027/cathode during turn ON.

Epoxy sealed RV8001 (at IC8001/pin 9) sets the shutdown threshold. When the HV is correctly set at 31.5kV, the resultant voltage a test point CN5506/pin 2 is between 4.36–4.66Vdc.

Excessive Current Protection

Excessive current drawn along the +200V line into this HV Converter stage will also feed the latch transistors (Q6530 and Q6532) directly, causing the TV to shut down. When this TV shutdown occurs, there is NO Standby light blink indication. The +200 line feeds IC8002, the two converter transistors (not shown) and the flyback transformer. Excessive HV will also cause the TV to shut down by drawing too much current through the flyback.

Excessive Beam Current (ABL)

Excessive current through the flyback transformer will stop the HV and shut down the TV if the HV current drain is excessive due to a failure. Such a failure can be due to shorted video output ICs, defective CRT or shorted FBT. When the ABL voltage from the FBT is excessive, Q8008 outputs a HIGH that exceeds 5.1Vdc at latch IC8001/pin 11. IC8001 outputs a HIGH at pin 13 that passes through D8027 to trip the latch that shuts OFF the TV.

In summary, shutdown without a Standby light indication indicates a problem is either in this HV stage or in the shutdown circuit itself.

HV Adjustment

The adjustment procedure for these three controls is straightforward. First, the shutdown controls are preset (ineffective). Then the RV8002 HV control is set to the shutdown trip point. The two shutdown controls are reset. Finally, the HV control is set. A HV probe connected to a DVM is required for this precise adjustment procedure.

The procedure is as follows:

1. Replace RV8001 and RV8002 (they are epoxied).
2. Turn RV8001 both CCW from the top of the D board.
3. Turn the set ON with a black screen (HV unloaded).

4. Adjust HV RV8002 for 35.5kV (shutdown threshold). Use an accurate DVM with HV probe.
5. Adjust RV8001 until the set just shuts down.
6. Turn HV RV8002 CW to turn the set ON. Input a white signal. Bring the HV up to 35kV to make sure the set does not shut down. (This rechecks the RV8001 adjustments.)
7. Adjust HV RV8002 for 31.5kV.

Testing

1. HV Check - Measuring the voltage at D8025/Cathode verifies HV. Normally D8025/Cathode = 31.6Vdc when there is HV, and 0V when HV is missing. D8025's Anode voltage should not be higher than 0.6Vdc in normal operation (measured). D8025 is located next to the potted (epoxy sealed) RV8001/RV8003 controls at the left edge of the D board. See Figure 9-3 below:

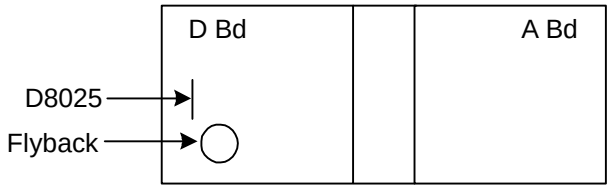


FIGURE 9-3 - KD34XBR2 rear

2. HV Converter Check - If no HV is output, look for +200V input at IC8002/pin 18 and more than 15.6V at IC8002/pin 8.

Look for HV Conv start voltage at IC8002/pin 1 (normally 1.6Vdc but must be more than 1.3Vdc. to start). See Charts 9-2 and 9-3 below:

Chart 9-2 - Converter IC8002 Voltages									
Pin	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
Volts	1.63	1.75	2.25	2.47	0	0	4.56	14.7	0
Pin	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**
Volts	10.3	0	4.14	0	108	98.6	103	0	200

Chart 9-3 Additional Important Voltages related to IC8002/pin 1 Voltage		
Electrical Location	Physical Location	Voltage
IC8001/pin 1	14 pin Surface mounted IC under RV8001/RV8003	0V
IC8001/pin 2		0V
C8004/ + lead	Behind IC5515's large heat sink next to large 820uf, 250V C8023.	0.02V

3. HV may be starting, then shutting down - Monitor D8025/Cathode for 31.6V at start up. If it is 0V, there is no HV. Check the converter transistors and suspect IC8002 and the flyback to cause OCP shutdown (via Q8009). If the cathode voltage momentarily rises beyond 31.6Vdc, there is HV but it may be excessive. Turn the RV8001 and RV8003 controls CCW and adjust the HV. Follow the HV adjustment procedure. If shutdown still occurs suspect D8025, C8005 and D8004.

Communications (HA-3 & RA-5A Chassis)

There are three communications buses in the HA-3 Direct view chassis (Figure 10-2) and similar RA-5A projection TV chassis (Figure 10-3):

- RXD/TXD bus between the Q box and the Main Micro (B board).
- S data and clock bus between the Main Micro and its TV operation ICs.
- B data and clock bus between the Main Micro and its memory ICs (NVM).

See Figure 10-1 below.

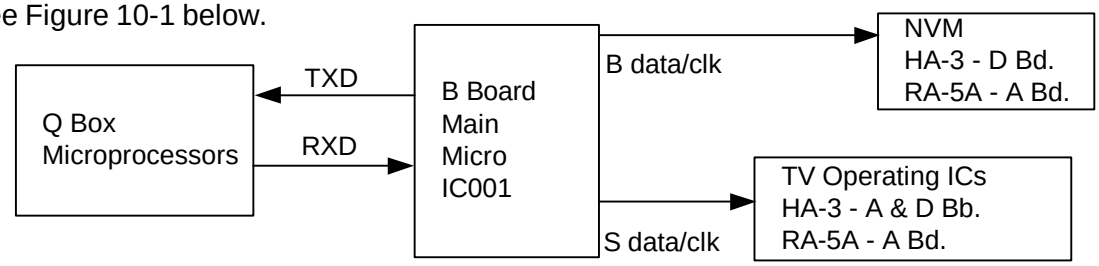
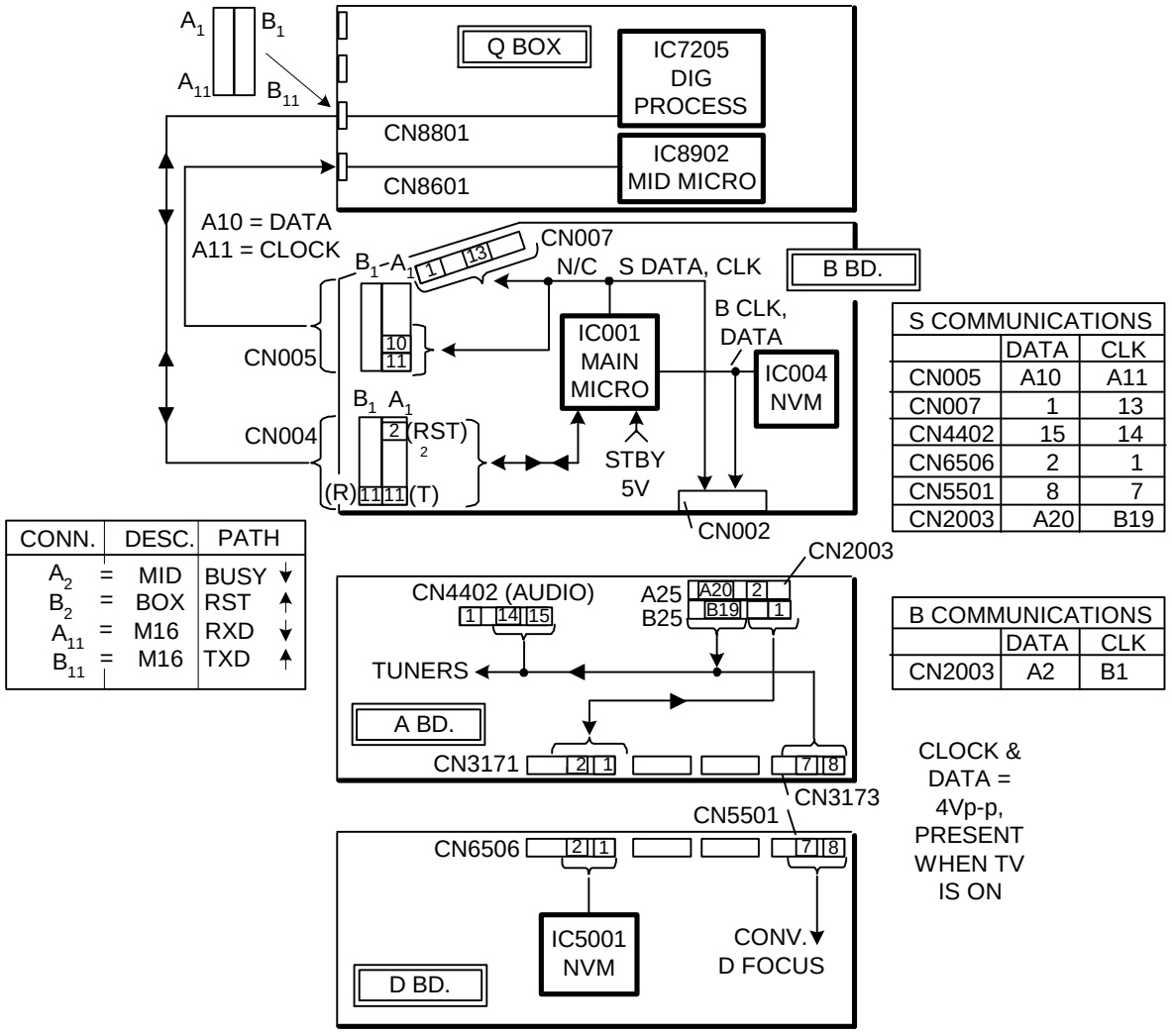


Figure 10-1

In comparing the two chassis, the only communication differences between them are the final destinations of the two buses on the A and D boards.



CONN.	DESC.	PATH
A_2 =	MID	BUSY ↓
B_2 =	BOX	RST ↑
A_{11} =	M16	RXD ↓
B_{11} =	M16	TXD ↑

S COMMUNICATIONS		
	DATA	CLK
CN005	A10	A11
CN007	1	13
CN4402	15	14
CN6506	2	1
CN5501	8	7
CN2003	A20	B19

B COMMUNICATIONS		
	DATA	CLK
CN2003	A2	B1

FIGURE 10-2 - HA-3 CHASSIS COMMUNICATION

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RXD/TXD bus

Normal Operation

The individual RXD and TXD lines are active at:

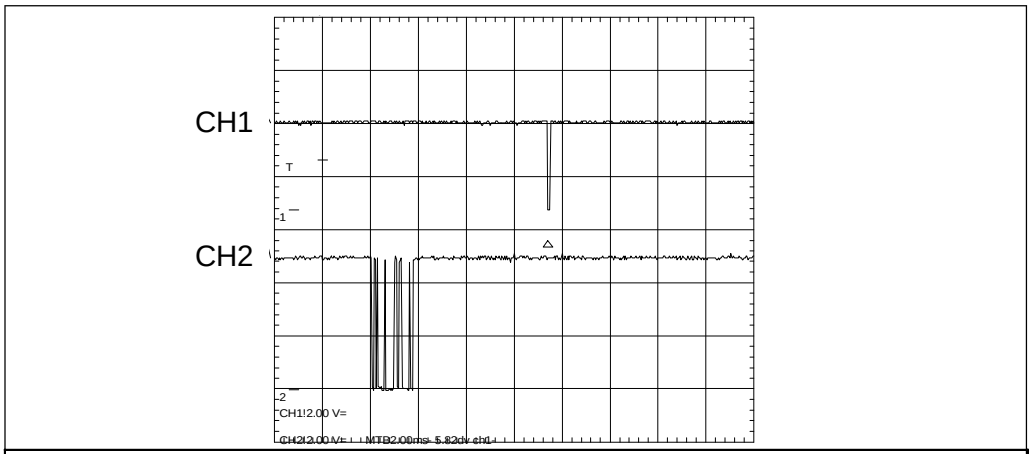
- TV power ON,
- The end of a microprocessor program (periodic activity), and
- When the Q box is needed.

At power ON, there is bi-directional communications between the Main Micro (IC001) on the B board and the Digital Processor in the Q box.

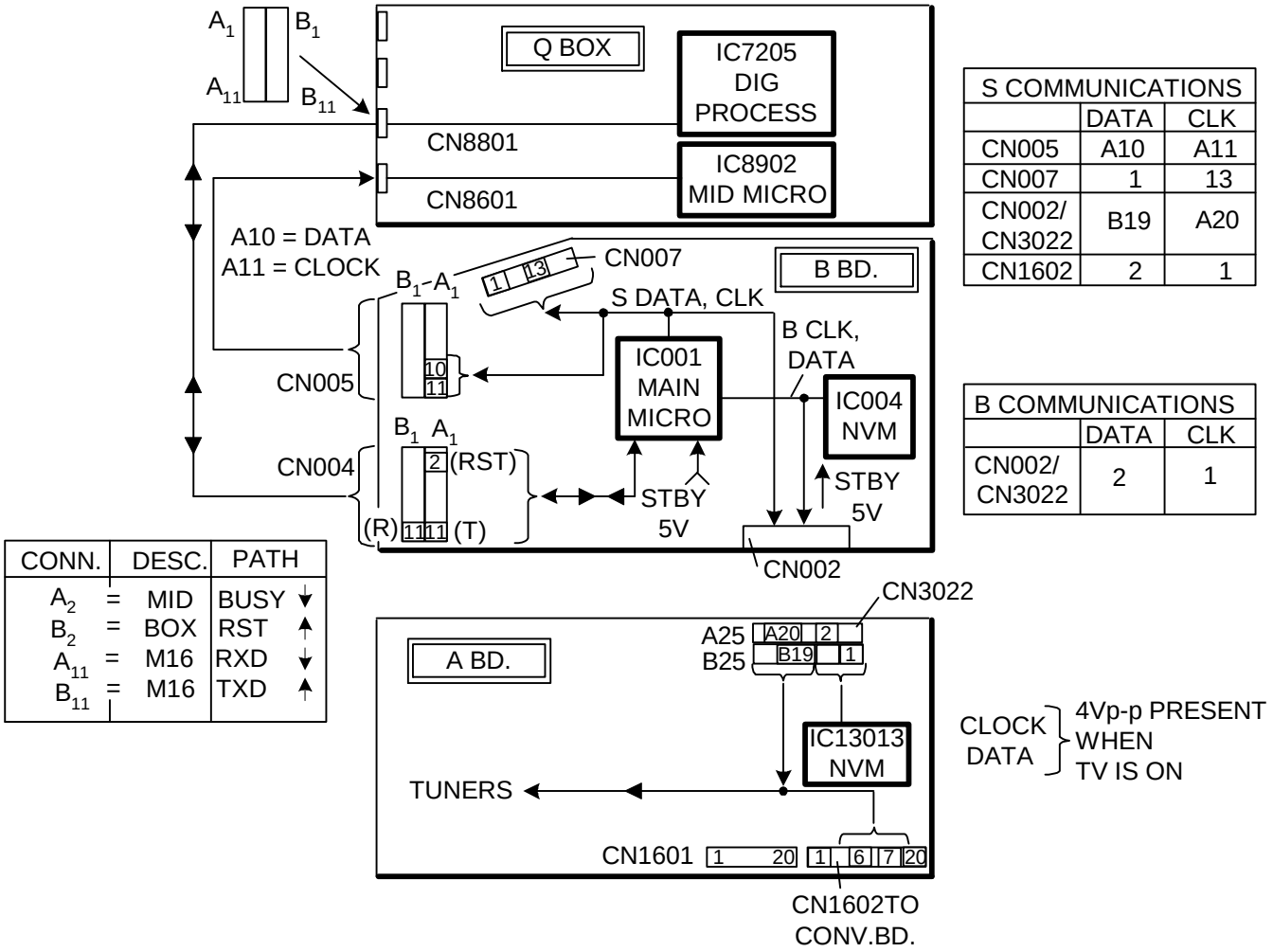
After power ON in normal operation, there is periodic communications on the TXD/RXD lines initiated by IC001 that results in just an acknowledgment (RXD) pulse. Communications is also present when changes to the Q box operation are called for, as shown in Waveform 10-1. Note that the normal output of IC001 is 5Vp-p and the reply signal from the Q box is only 3Vp-p because of their operating B+ levels.

While the TV is operating, there is only periodic communications when required. Waveform 10-1 shows typical Q box to Main Micro IC001 (B Bd) bi-directional communications. This waveform was taken when changing into a DTV station (channel up command).

In the waveform sequence below, notice that the Main Micro starts the communications (ch 2) and the Q box micro replies afterwards (ch 1). When changing into NTSC stations the Q box does not have to select a station so there is no (ch 1) reply (acknowledgment).



Waveform 10-1 – Microprocessor Communications* QM – B Board			
Channel	Signal Name	Location	Vp-p
1	RXD to Main Micro IC001 (B Bd)	CN8801/pin B11	3Vp-p
2	TXD	CN8801/pin A11	5Vp-p
Time Base = 2msec/div.			
* Taken when channel changing into a DTV station. When changing to another NTSC station, RXD signal (ch 1) from the Q box is not present.			



S COMMUNICATIONS		
	DATA	CLK
CN005	A10	A11
CN007	1	13
CN002/ CN3022	B19	A20
CN1602	2	1

B COMMUNICATIONS		
	DATA	CLK
CN002/ CN3022	2	1

CONN.	DESC.	PATH
A_2 =	MID	BUSY ↓
B_2 =	BOX	RST ↑
A_{11} =	M16	RXD ↓
B_{11} =	M16	TXD ↑

FIGURE 10-3 - RA-5A CHASSIS COMMUNICATIONS 53TVP12 1365 9/6/01

Loss of RXD/TXD Communications

Symptom 1 - Loss of RXD/TXD Communications between the Q box and the Main Micro results in a white screen with no sound as if there is a break in the video path. This is because the Q box has no instructions (communications) to configure the video ICs within the Q box so there is no active video output.

During this RXD/TXD Communications failure, the B and S data/clock communications is still active as long as the TV is ON. This means main TV micro still communicates with the NVM ICs and TV operation ICs so the TV deflection stages are working even though there is no audio and video.

Symptom 2 - If the power to the Q box is removed, the TV responds to the power ON/OFF button but the screen is dark with no audio. The B and S data/clock communications is still active without the Q box power.

S data and clock bus

This data bus is bi-directional with the video processor on the A board (and AD board in the RA-5A projection TV chassis), but unidirectional with the remainder of the ICs in the TV. The clock signal comes from Main Micro IC001. Both data and clock signals are 4Vp-p and are always present as long as the TV is ON. This output drops to 2Vp-p if the Q box power was removed (CN7001 unplugged).

B data and clock bus

This data bus is a bi-directional bus connecting the Main Micro IC001 with the two Non-Volatile Memory (NVM) ICs. The data and clock lines are 4Vp-p and are always present as long as the TV is powered ON.

On Screen Displays

The main (white) menu comes from the Digital Processor Micro within the Q box. The menu data is sent on an EMI communications bus used solely within the Q box to its OSD IC, which is also within the Q box.

The green service mode OSD, channel numbers and user functions (e.g. volume, picture) come from the Main Micro IC001 on the B board. IC001 communicates with the Q box for this purpose using RXD and TXD as explained above. The OSD RGB output is applied to the video processor IC on the A board.

The white crosshatch patterns and dots OSD used for convergence in the projection TV set (RA-5A chassis) comes from the AD board. The OSD RGB output is applied to the video processor IC on the A board.

Video Process (HA-3 & RA-5A Chassis)

The bulk of the video process is the same for the HA-3 and RA5A chassis. The differences are the connector numbers on the A boards. Therefore this video process section applies to both chassis and contains:

- Overall Video Block
- Overall Sync Path
- Board Replacement Repairs
- Component Level Repair

Sony's direct view HA-3 TV chassis drives a 16x9 flat-faced picture tube. The acceptable inputs for this chassis are listed in Chart 11-1. Refer to Figure 11-1 for the video signal flow that follows.

Chart 11-1 – HA-3 Input	
TV Input	Acceptable Input
DTV TV stations	Air Channels 1-99 in 18 ATSC digital formats
Analog TV stations	Air (ch 2-69) or cable (ch 1-125) in the NTSC analog format
Video 1-4	S or composite video in standard 480i format (525 line)
Video 5-6	Y, Pb, Pr component video in 480i, 480p, 720p, or 1080i format

A general description of the video flow by board is explained for each of the four input groups.

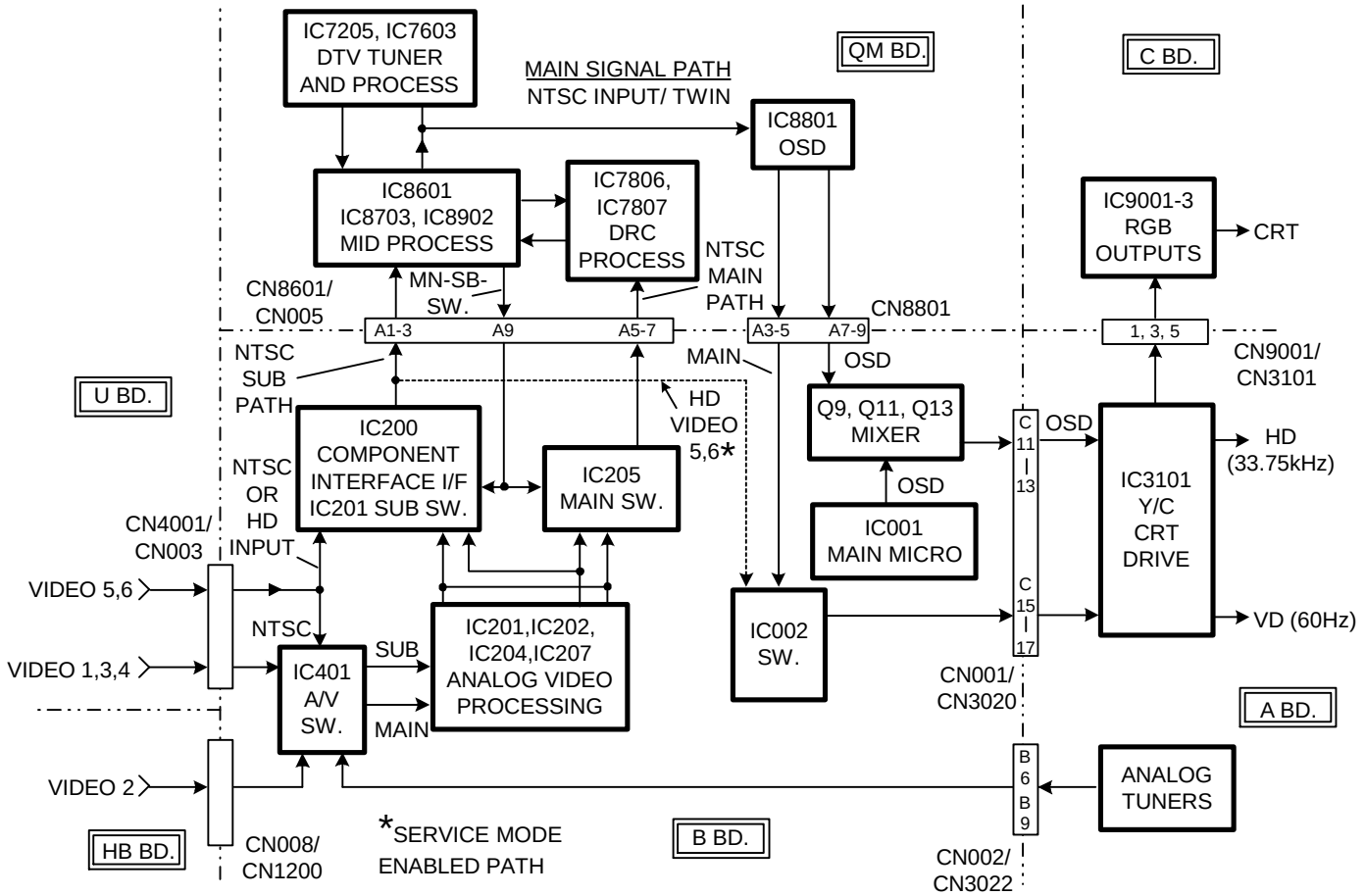


FIGURE 11-1 - VIDEO BLOCK - HA-3 CHASSIS

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Digital TV station Input

QM board – Selecting a digital TV channel requires the communications of the Main Micro IC001 (B board) and Digital Processor IC7205 (QM board - not shown). At each channel up or down command, the Main Micro IC001 (B Bd.) asks Digital Processor IC7205 if the next station is an active DTV station. If the next station is digital, the reply contains the channel number (IC001 displays channel numbers). Main TV Micro IC001 instructs IC7205 (QM board) to receive that DTV channel.

Digital TV station processing is then entirely performed on the QM board. The DTV tuner receives the station while its circuitry (IC7205, IC7603) converts the digital signal to final component video form with two or six channel audio output. OSD IC8801 buffers the component analog video before sending it to the B board.

Previously, the TV's Main Micro generated the OSD menu and channel numbers. IC8801 now generates all the TV menu graphics from the QM board, but the Main Micro (B board) still makes the green channel numbers and controls the service mode display.

B board – The menu OSD from IC8801 (QM board) and channel number/service mode OSD from the Main Micro IC001 are combined by Q9, Q11 and Q13 and sent to the A board. The DTV's component video passes through switch IC002 and enters the A board.

A board – Both the OSD information (if any) and the DTV station's component video enter the Y/C, CRT Drive IC3101 to be merged. The combined output leaves as RGB to the CRT on the C board.

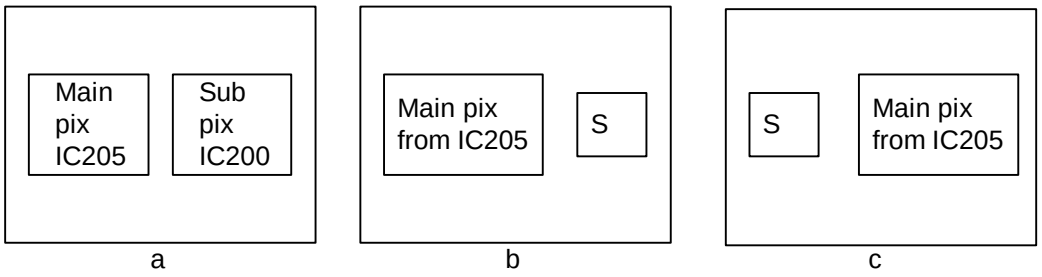
Analog TV station Input

A board – Both the main and sub analog tuners are mounted on the A board. Their composite video outputs are sent to the A/V switch on the B board.

B board – A/V switch IC401 chooses the signal path for the main and sub tuners. The main tuner signal may either enter the main path or be switched into the sub path. The main path leaves IC205 on the B board for the QM board (Q Box). The sub path leaves IC200 on the B board for the QM board (Q Box). When a single analog picture is selected, the main signal path into the DRC circuitry on the QM board is always taken, no matter which tuner originates the signal.

In the Twin View picture mode (Figure 11-2), both main and sub paths are used to produce two pictures on the screen side by side. The main picture from IC205 is positioned on the left side by the MID circuit when both pictures are the same size (Figure 11-2 a) or the left picture is the larger picture (Figure 11-2 b). When the picture on the right becomes the larger (Figure 11-2 c), the MID process reverses the position so the larger picture always comes from the DRC process (main signal path) via IC205. Earlier in the signal path, IC200 and IC205 switch the input signals to keep the same station at the same position on the screen. The main (IC205) and sub (IC200) IC switches are inversely controlled by a single "MN SB SW" line from the MID micro on the QM board. A slight delay occurs when the right picture just begins to become larger, allowing the MID circuit to switch positions. The picture freezes for a moment until both switches have been made, then the frame continues to increase in size.

Figure 11-2 - Twin Picture Mode, Analog Inputs



QM board – The main and sub video signals are both input to the MID circuitry, but the Main signal passes through the DRC circuit first. The DRC circuit increases the number of pixels of the standard resolution NTSC signal. The MID circuit selects one of three inputs (DTV, sub video, main video), then changes its input horizontal frequency (see Chart 11-2 for the possible input frequencies) and the aspect ratio to match the TV parameters. The TV horizontal frequency is always 33.75kHz.

Chart 11-2 – Input signal H. Frequency	
Input signal	Horizontal Frequency
Standard NTSC 480i	15,734 Hz
High Resolution 480p	31.5kHz
High Resolution 720p	45.kHz
High Resolution 1080i	33.75kHz

The MID circuit output is high-resolution component video and separate H & V sync lines. The OSD IC buffers the video before leaving the QM board.

B board – CN004 receives the video signal and SW IC002 on the B board acts as a pass-through for the video signal. The video leaves unaltered at CN001 (see Figure 11-3) into the A board.

A board - Both component video and sync leave the B board and enter the Y/C CRT Drive IC on the A board. From the A board, the RGB signal is applied to the CRT cathodes.

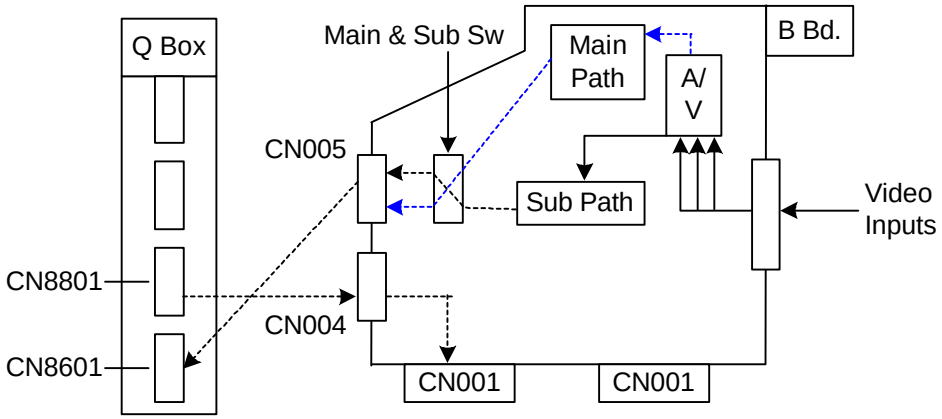


Figure 11-3 - HA-3 & RA-5A Video Path

Video 1-4 Input

Composite video from video inputs 1-4 enter the U or front panel HB board and pass through the A/V switch IC401 on the B board. From there, they take the same path as explained in the Analog TV stations.

Video 5-6 Input

U board – The U board houses the component video input jacks (Y, Pb, Pr). The signal is input to the B board.

B board – The component video signal enters component interface switch IC200 and goes into the QM board.

QM board – The MID process (IC8601, IC8703) converts the 480i, 480p, 720p or 1080i video format and separate sync frequencies to 540p/1080i (video) and 33.75kHz (H sync) to match that of the TV. The component video output is sent through IC8801 into the B board. The sync is sent through the B board into the A board (not shown).

B board – The component video passes through IC002 and goes to the A board. Switch IC002 is not normally used as a switch except when enabled using the service mode. Then a 1080i video 5, 6 signal can be made to avoid the QM board for testing purposes. See Video Adjustments for the procedure.

A board – The Y/C CRT Drive IC3101 converts the input video to RGB, mixes any OSD and outputs the combined signal to the CRT on the C board.

In the twin picture mode, the DTV picture or video 5 or 6 high resolution input will always appear on the left side and never swap places. Video 5, 6 or a DTV station CANNOT be selected in the right picture.

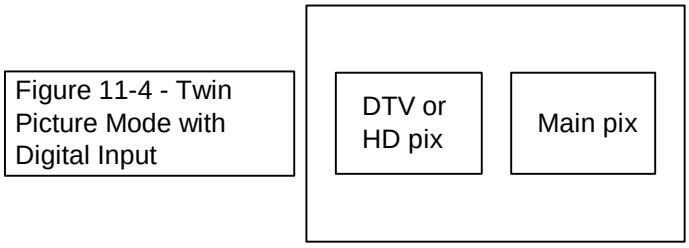


Figure 11-4 - Twin Picture Mode with Digital Input

Overall Sync Path

The sync paths for the analog and digital TV tuner and video inputs are shown in Figure 11-5. The sync is first stripped from the video on the left B board. Both the main and sub sync signals input the QM board as NTSC standard, but leaving is 33.75kHz to match that of the TV's horizontal oscillator frequency. Normally switch IC006 on the right part of the B board just passes the 33.75kHz from the (QM board's) MID circuit. IC6 only selects the sub path sync when the HD High Pass mode is selected from the service mode. See the Conv. Adjustments Overview section for details.

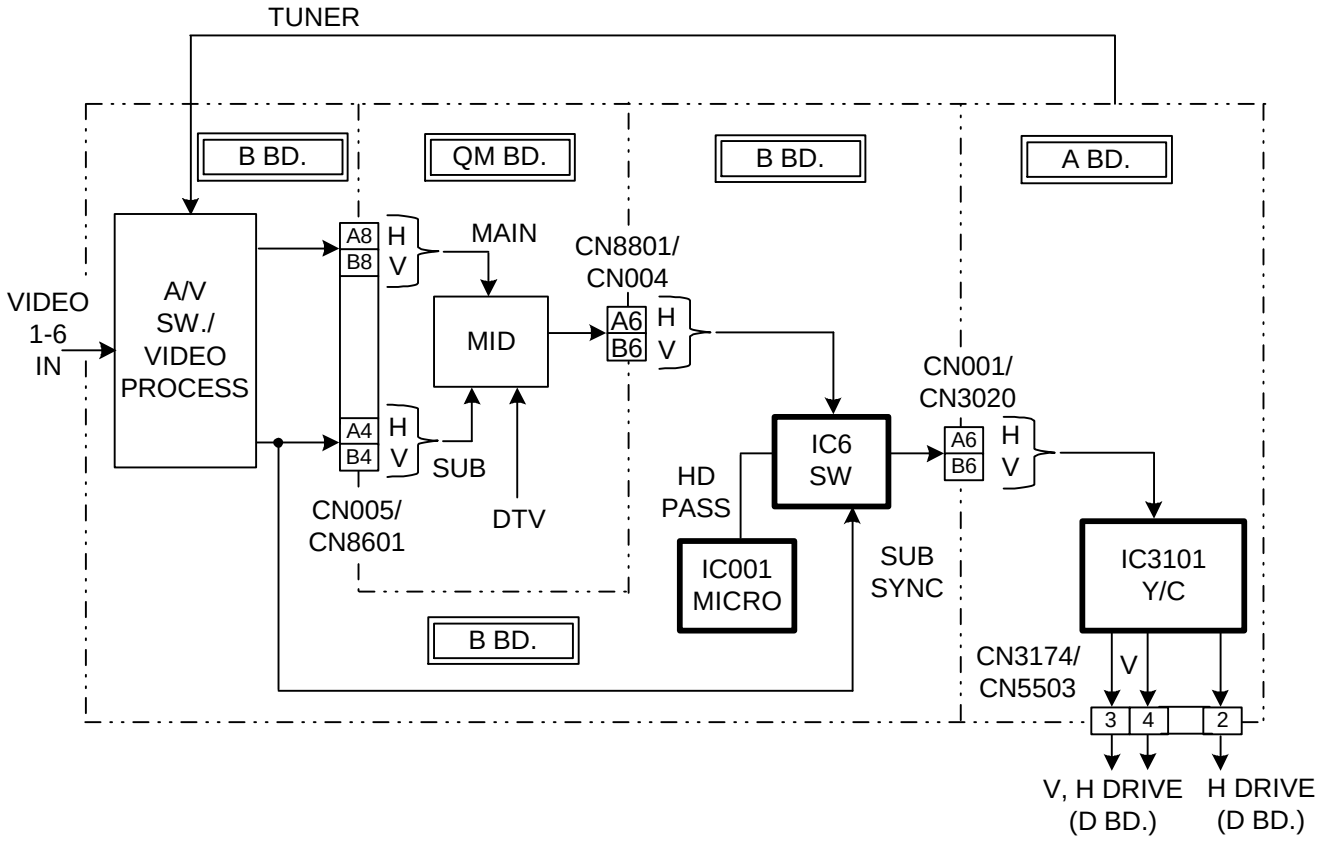


FIGURE 11-5 - HA-3 SYNC PATH

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Chart 11-3 - Horizontal Sync Levels – Input is 15.735kHz NTSC at Video 1				
Location	Board	Description	Frequency	Vp-p
CN005/pin A8	B	Output - Main H from B board	15.735kHz	3.5Vp-p
CN005/pin A4	B	Output - Sub H from B board	15.735kHz	3.6Vp-p
CN8801/pin A6	QM	Output – Pix sync from MID circuit	33.75kHz	3.7Vp-p
CN001/pin C18	B	Output – Final pix sync from QM bd or Video 5 or 6, 1080i input signal	33.75kHz	5Vp-p

Board Replacement Repairs

The following are very simplified signal flow diagrams used to quickly see the Main, Twin and HD signal paths for board isolation. The paths are the same in the HA-3 and RA-5A TV chassis because they use the same B and Q box that houses the bulk of the video signal processing.

Main Video Path

When a single picture is chosen from the analog tuner or video inputs, the path shown in Figure 11-6 applies.

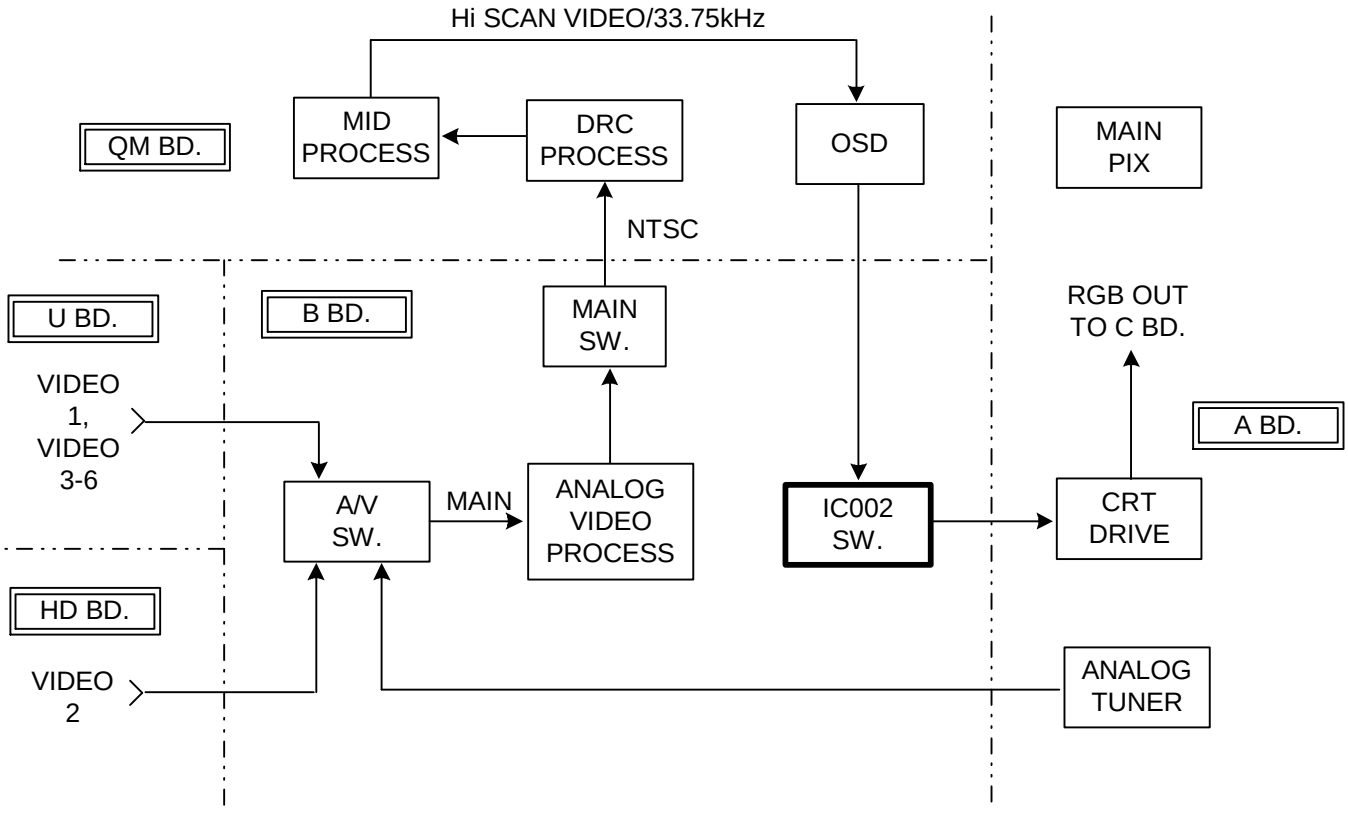


FIGURE 11-6 - NTSC MAIN PIX VIDEO PATH 8TVP12 1325 9/4/01

Only the main signal path is used to direct the analog composite video from the rear panel (U board) or main tuner (A board). Component video (Y, Pb, Pr) with H & V sync lines is sent to the QM board for conversion into a high resolution, high frequency video signal to match that of the TV.

The OSD IC buffers the component video signal before leaving the QM board and returning to the B board. SW IC002 on the B board acts as a pass-through for the video signal. Both component video and sync from the QM board leave the B board and enter the Y/C CRT Drive IC on the A board. From the A board, the RGB signal is output to the CRT cathodes.

NTSC Twin View (Picture with Picture) Video Path

When the Twin View (Picture with Picture) feature is selected, two pictures appear on screen side by side. Two video sources are chosen and two video paths are used to support these pictures. The main picture starts at the left side when the pictures are the same size. With the remote, one picture can be made larger than the other can. The larger picture will always take the main picture path with two NTSC inputs so video paths are switched as necessary. Picture switching is done at the MID Process (QM board) and the Component I/F and Main Sw ICs on the B board.

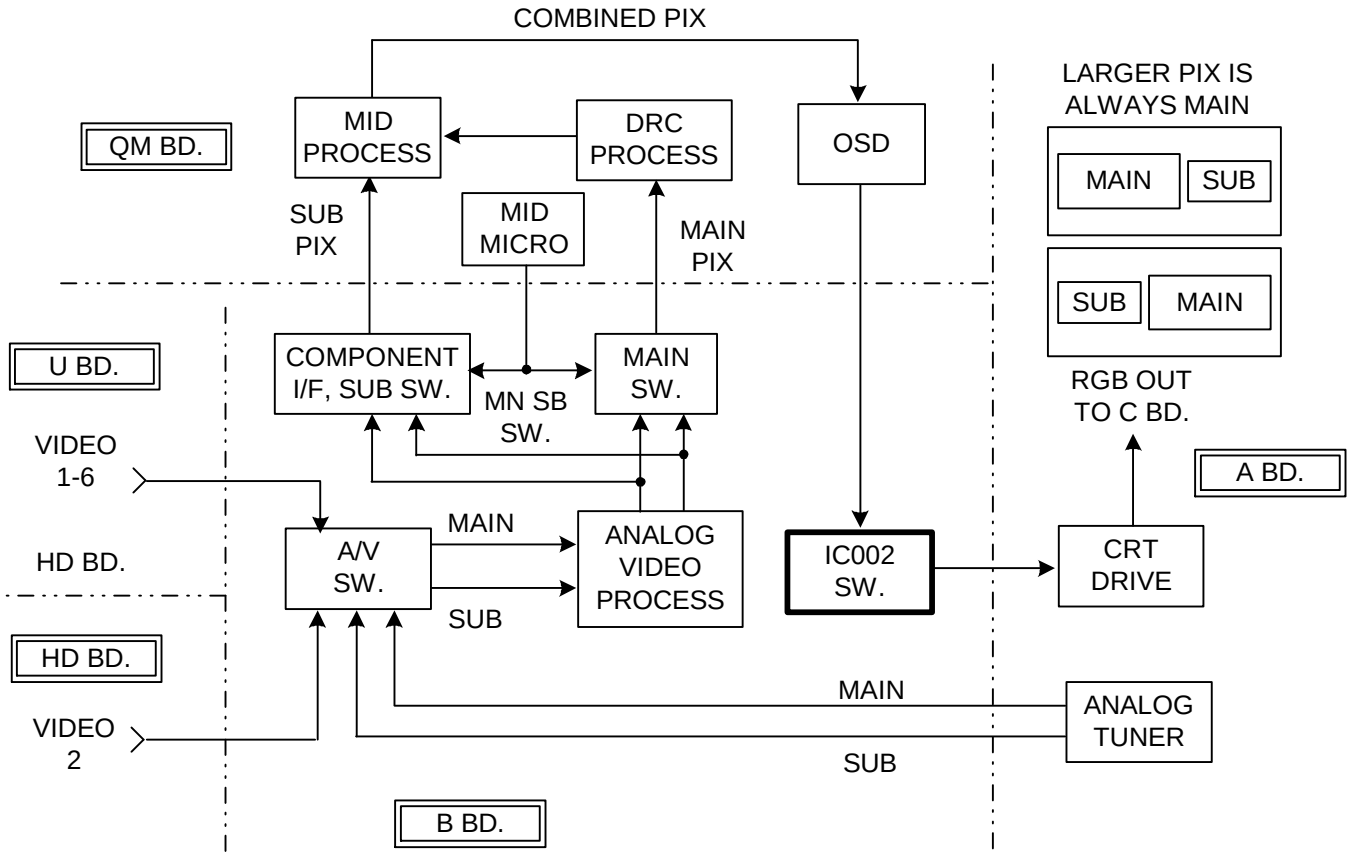


FIGURE 11-7 - NTSC ONLY TWIN VIEW VIDEO PATH 9TVP12 1326 9/4/01

The combined picture leaves the MID process with a new horizontal frequency to match the TV as well. An OSD IC buffers the component video before leaving the QM board. The component video and sync pass through the B board and enter the Y/C CRT Drive IC on the A board. The Y/C CRT Drive IC output is RGB that goes into the C board and CRT cathodes.

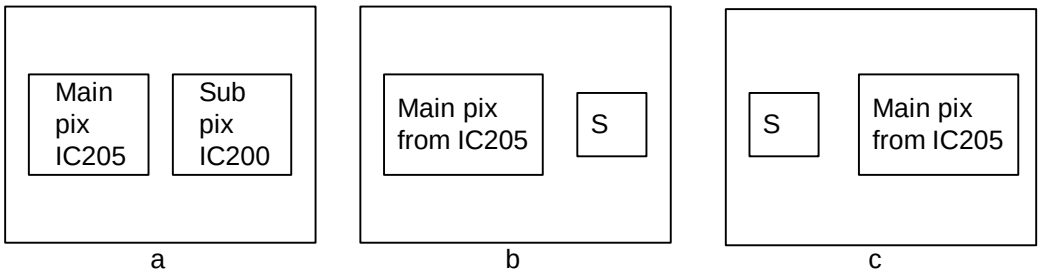
Main and Twin Mode Video Troubleshooting

Because of the switching in the Twin mode, we can use the Twin Mode user operation to isolate the problem to a board. Use Figure 11-8 for identifying a video problem using two NTSC signals, and Figure 11-13 for an ATSC signal problem. With the suspected board in mind, you can use your scope to prove the problem is in the suspected board by checking for video signals at chassis connectors (signal tracing).

Flow Charts for locating a defective board

In the Twin Picture Mode the main picture video signal path is always used to display the largest picture. To do this the MID circuit in the Q box and switching ICs on the B board may interchange paths depending upon which picture is the largest. Use the flow charts to change the size of the pictures in Twin Mode and isolate the problem to a board.

Figure 11-2 - Twin Picture Mode, Analog Inputs



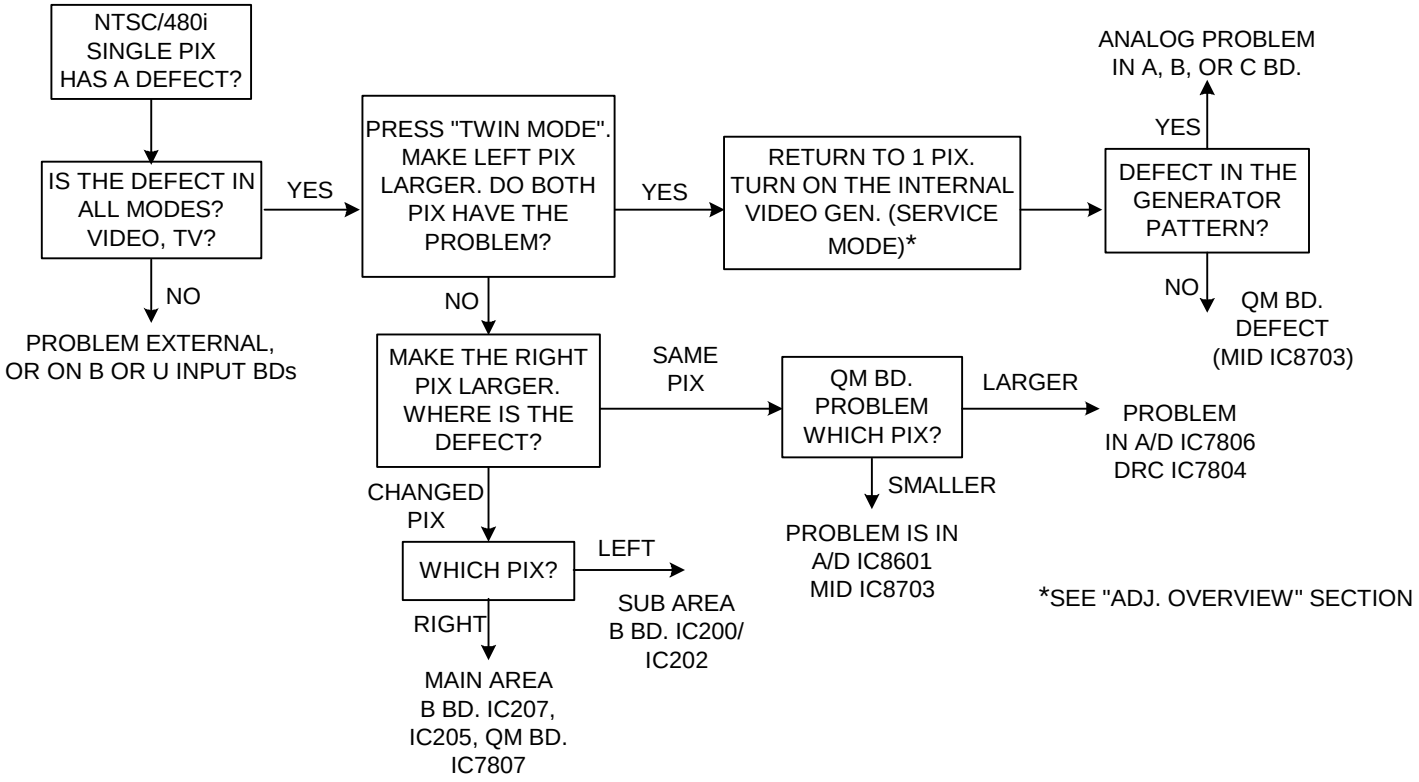

NTSC/480i SINGLE PIX HAS A DEFECT?
IS THE DEFECT IN ALL MODES? VIDEO, TV?
YES
NO
PROBLEM EXTERNAL, OR ON B OR U INPUT BDs
PRESS "TWIN MODE". MAKE LEFT PIX LARGER. DO BOTH PIX HAVE THE PROBLEM?
YES
NO
RETURN TO 1 PIX. TURN ON THE INTERNAL VIDEO GEN. (SERVICE MODE)*
DEFECT IN THE GENERATOR PATTERN?
YES
ANALOG PROBLEM IN A, B, OR C BD.
NO
QM BD. DEFECT (MID IC8703)
MAKE THE RIGHT PIX LARGER. WHERE IS THE DEFECT?
SAME PIX
QM BD. PROBLEM WHICH PIX?
LARGER
PROBLEM IN A/D IC7806 DRC IC7804
SMALLER
PROBLEM IS IN A/D IC8601 MID IC8703
CHANGED PIX
WHICH PIX?
LEFT
SUB AREA B BD. IC200/ IC202
RIGHT
MAIN AREA B BD. IC207, IC205, QM BD. IC7807
*SEE "ADJ. OVERVIEW" SECTION

FIGURE 11-8 - FLOW CHART 2 - VIDEO TROUBLESHOOTING - NTSC PIX DEFECT 39TVP12 1355 8/30/01

Signal Tracing to prove the problem is on the board

Refer to the following to support the traditional video signal tracing in the HA-3 and RA-5A TV chassis:

- Figure 11-1 for the signal flow
- Figure 11-10 for the location of HA-3 chassis connectors.
- Chart 11-4 shows the Video Signal Levels along the way
- Waveforms 11-1 – 11-3 that show the signal shapes with an NTSC color bar input to the TV.

Conditions of measurement - Color bars are input to the main (VHF/UHF) and sub (Cable) tuners from two separate NTSC generators for ease of signal tracing. The color bar signal is followed as it enters and leaves a board. The Sub signal is always present at the connector even though it is not being used. The TV is tuned to Channel 3 and Channel C3.

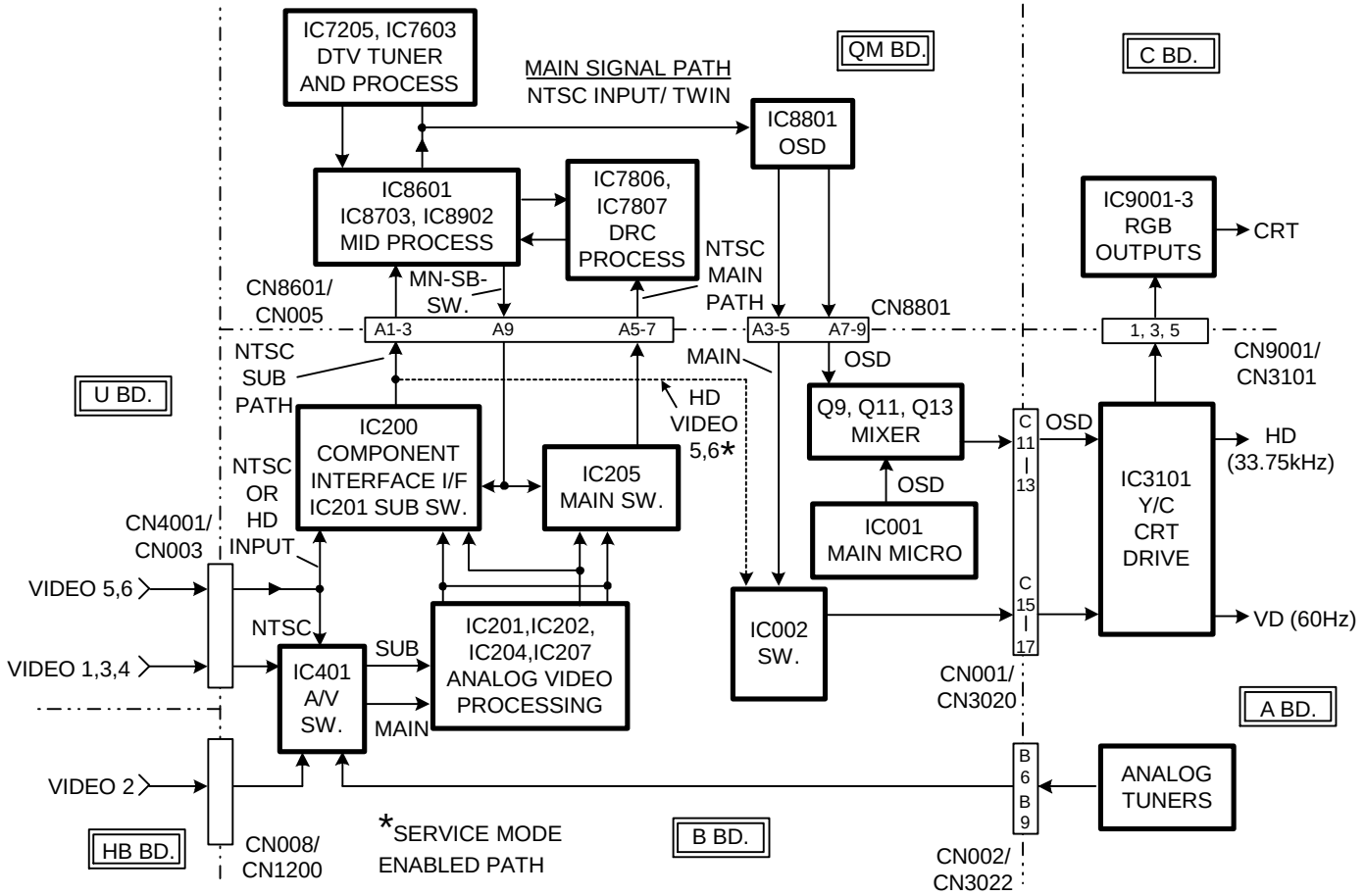


FIGURE 11-1 - VIDEO BLOCK - HA-3 CHASSIS

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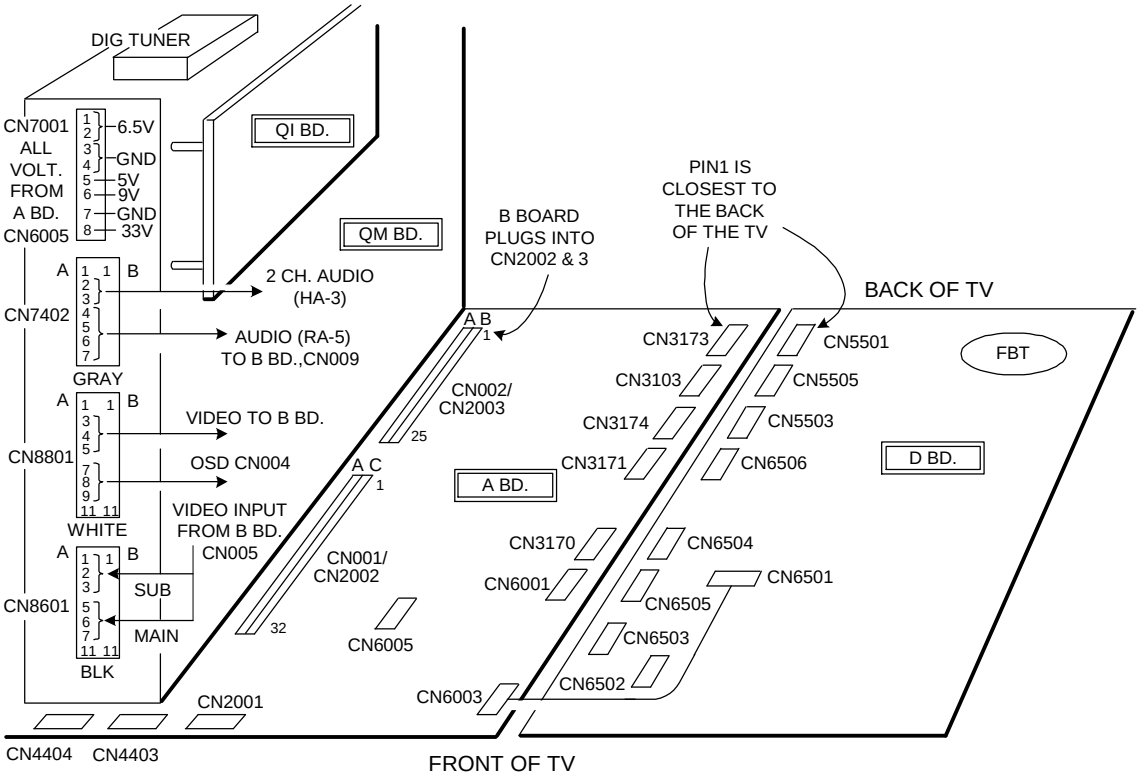

FIGURE 11-9 - HA-3 CHASSIS CONNECTOR LAYOUT

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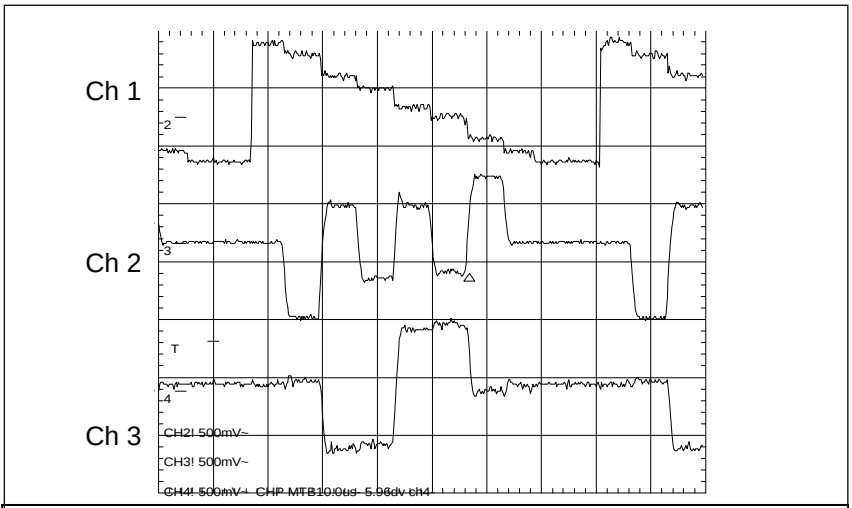
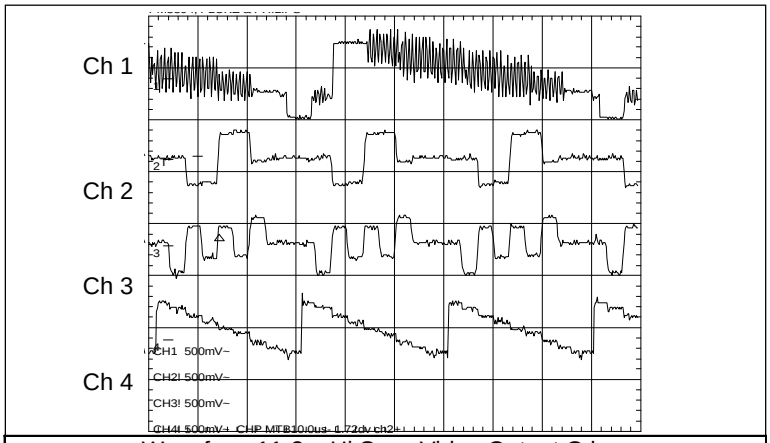
Chart 11-4 - Video Signal Levels - HA-3 Chassis, RA-5A Chassis Similar				
Signal Name	Location	Board	Voltage	
Main tuner output A bd.	CN002/pin B6	Input B	1Vp-p	Composite video bars (gen. 1)
Sub tuner output A bd.	CN002/pin B9	Input B	1Vp-p	Composite video bars (gen. 2)
Main Y Signal	CN005/pin A5	Output B	1Vp-p	NTSC Main Component video output the B board
Main Pb	CN005/pin A6	Output B	1.2Vp-p	
Main Pr	CN005/pin A7	Output B	1.2Vp-p	
Sub Y Signal	CN005/pin A1	Output B	1.2Vp-p	NTSC Sub Component video output the B board
Sub Pb	CN005/pin A2	Output B	1.2Vp-p	
Sub Pr	CN005/pin A3	Output B	1Vp-p	
Hi Scan Y Signal	CN001/pin C15	Input B	0.7Vp-p	High Resolution Component video output Q box
Hi Scan Pb	CN001/pin C16	Input B	0.6Vp-p	
Hi Scan Pr	CN001/pin C17	Input B	0.5Vp-p	
Menu	CN001/pin C12 (green)	Output B	0.5Vp-p	OSD white menu signal

Waveform 11-1 shows component video leaving the B board into the Q box. The main and sub signals look the same. Only the main output is actually shown.



Waveform 11-1 – Main / Sub Signal Output B Board			
	Name	Location	Voltage/div
Channel 1	Main / Sub Y	CN005/pin A5 / A1	1.2Vp-p
Channel 2	Main / Sub Pb	CN005/pin A6 / A2	1.2Vp-p
Channel 3	Main / Sub Pr	CN005/pin A7 / A3	1.2Vp-p
Time base	10usec/div		

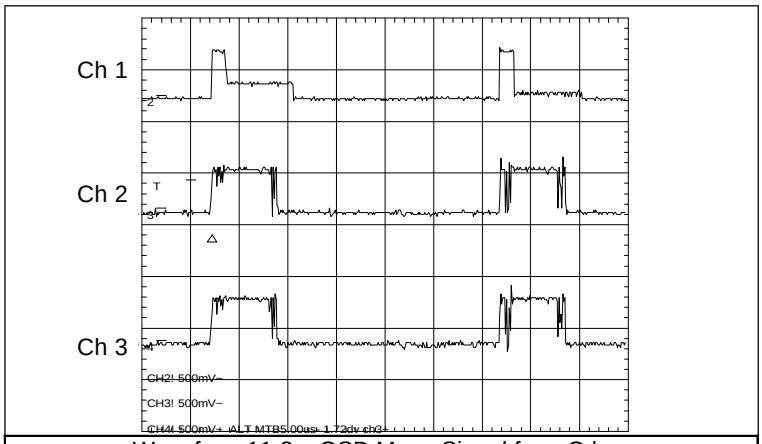
Waveform 11-2 shows the high-resolution output (ch 2-4) of the Q Box compared to the standard resolution (ch 1) color bar pattern composite input. The sync is doubled and the resolution is increased (density is higher).



Waveform 11-2 – Hi Scan Video Output Q box

	Name	Location	Voltage/div
Channel 1	NTSC Main Tuner Out	CN002/pin B9	1Vp-p
Channel 2	Hi Scan Pr	CN001/pin C17	0.5Vp-p
Channel 3	Hi Scan Pb	CN001/pin C16	0.6Vp-p
Channel 4	Hi Scan Y Signal	CN001/pin C15	0.7Vp-p
Time base	10usec/div		

Waveform 11-3 shows the menu signal output the Q box. This menu signal is present for 1.5 minutes after the menu button is pressed. The signal appears on all RGB outputs lines because the new menu is white in color. Cancel the menu by pressing the menu button again.



Waveform 11-3 – OSD Menu Signal from Q box

	Name	Location	Voltage/div
Channel 1	OSD Red	CN001/pin C13	0.5Vp-p
Channel 2	OSD Green	CN001/pin C12	0.5Vp-p
Channel 3	OSD Blue	CN001/pin C11	0.5Vp-p
Time base	10usec/div		

High Definition (HD) Video Path

A high definition signal can come from the DTV tuner in the QM board or externally from the TV's rear video 5 or video 6. See Figure 11-10 for signal flow to each board and Chart 11-5 for a video path list.

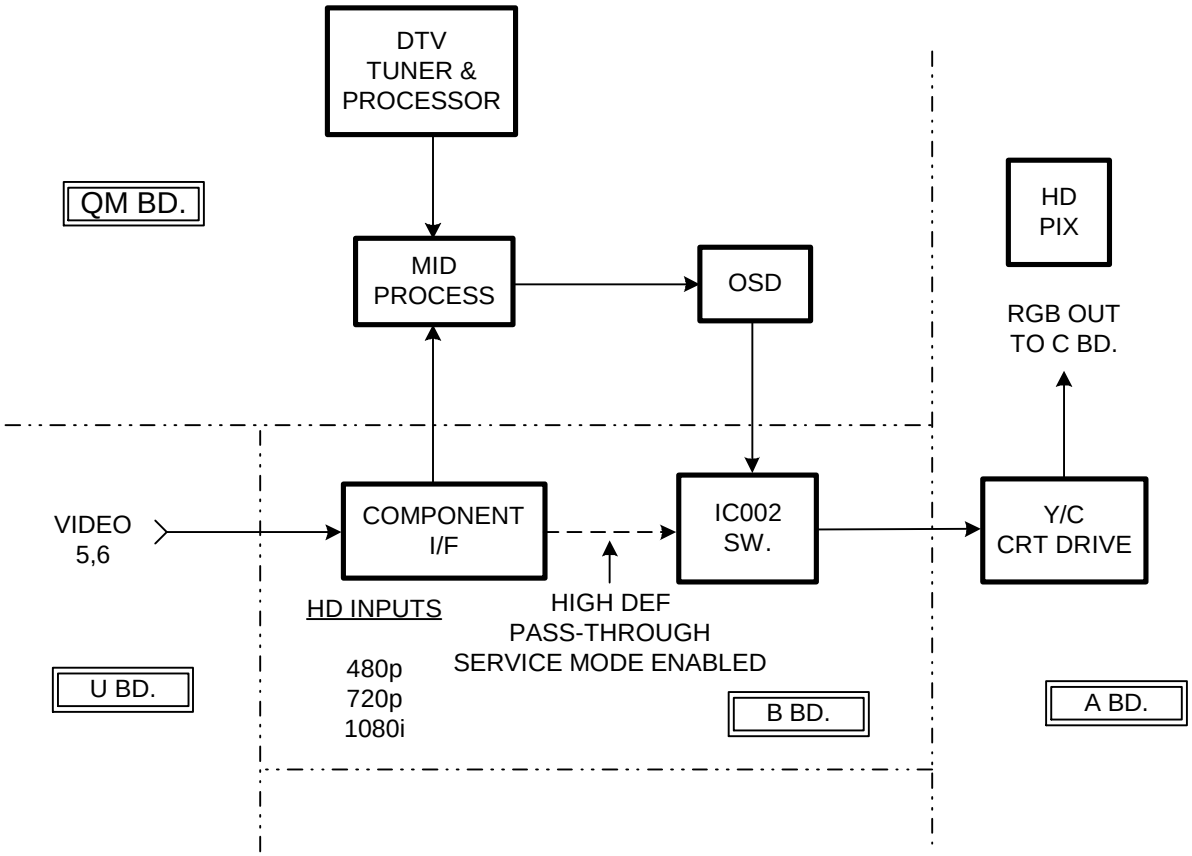


FIGURE 11-10 - HD VIDEO PATH 10TVP12 1328 8/30/01

Chart 11-5 - High Definition Video Signal Path					
Video 5 or 6 Input			DTV Air Signal		
Stage	Board	Purpose	Stage	Board	Purpose
Input	U	Input	DTV Tuner	QM	DTV Reception
Component Interface IC200	B	Video buffer; H & V Sync extraction	DTV Process	QM	Decodes one of 18 ATSC formats. Input = Antenna Outputs = component video.
MID Processor	QM	Signal determination based upon sync freq.; aspect ratio change; H freq. change to 33.75kHz	MID Processor	QM	Signal determination based upon sync freq; aspect ratio change; H freq. change to 33.75kHz. Combines pix.
OSD	QM	Video buffer, User Menu OSD	Combined with the Video 5 or 6 picture by the MID Processor		
SW IC002	B	Video Pass through			
Y/C CRT Drive	A	Input = Component Video. Output = RGB. Adds Menu OSD from QM board.			

HD Twin View (picture with Picture) Video Path

When a HD signal from the DTV tuner or Video 5 or 6 input is selected in Twin View, this HD picture will remain fixed at the left side of the screen. The signal path is easy to see in Figure 11-12 and the signal path is listed in Chart 11-6.

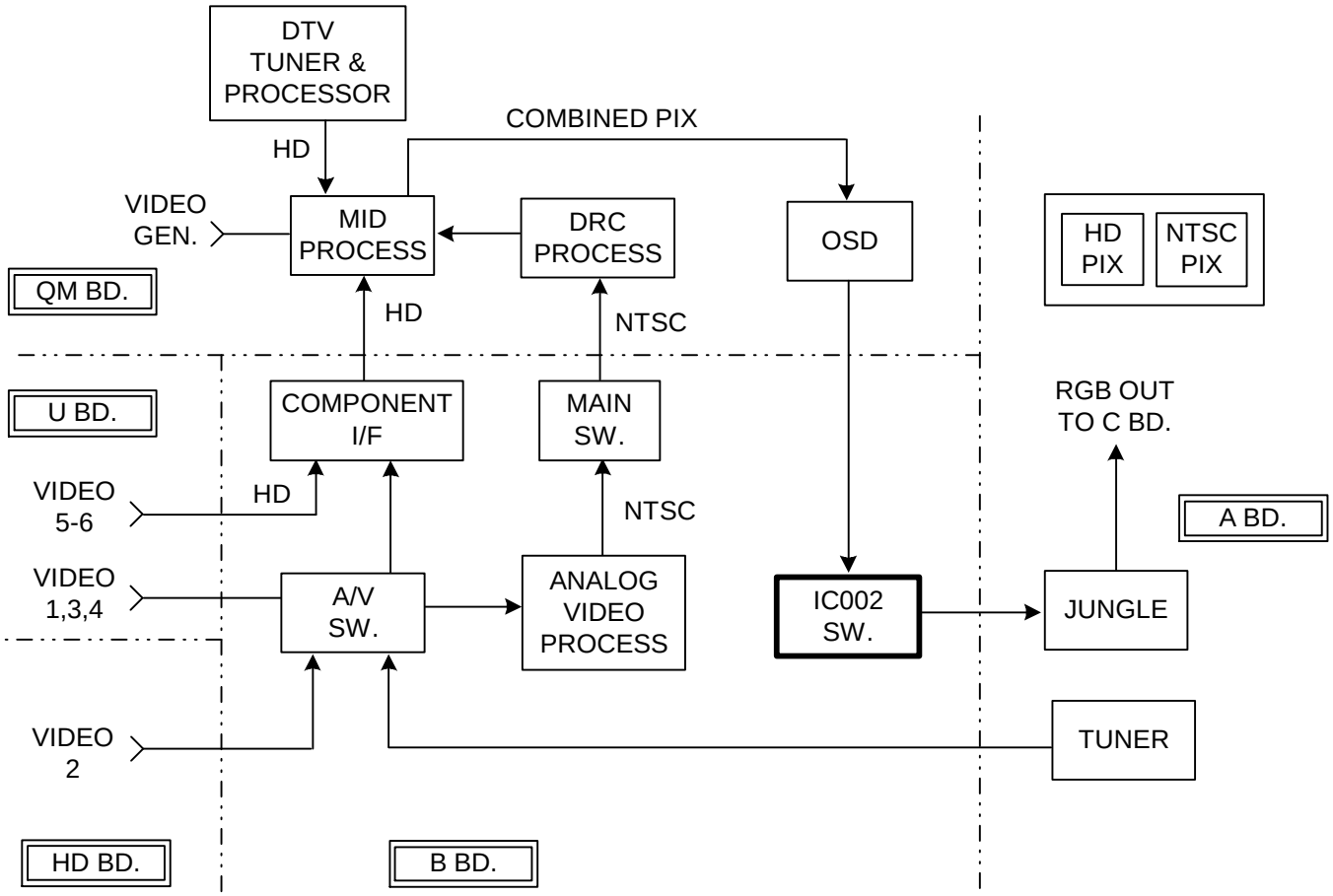


FIGURE 11-11 - HD & NTSC TWIN VIEW VIDEO PATH 11TVP12 1327 8/30/01

Chart 11-6 - HD Twin View Video Signal Path					
HD Signal Path			NTSC Signal Path		
Stage	Board	Purpose	Stage	Board	Purpose
DTV Tuner	QM	Input = Outside Antenna Output = Component Video	Main NTSC Tuner	A	Receives cable, or off the air TV stations
Video 5, 6	U	Video Input	A/V Switch	B	Selects NTSC input
Component Interface	B	Video buffer; H & V Sync extraction. Output = Video & Sync	Analog Video Process	B	Inserts closed caption, Detects ID1 aspect ratio signal, parent control. Input = composite video Output – Component video & sync (not shown)
DTV Tuner & Process	QM	Decodes one of 18 ATSC formats. Input = Antenna Outputs = component video.	Main Switch	B	Remains locked to the main signal input
MID Processor	QM	Selects Video 5/6 or DTV input; H freq. change to 33.75kHz.	DRC Process	QM	Increases the pixel number.
MID Processor	QM	Creates two pictures on the screen.	MID Processor	QM	Creates two pictures on the screen.
OSD	QM	Video buffer, User Menu OSD	The MID Processor combines with the HD picture with this input on the screen.		
SW IC002	B	Pass through only. Switch is disabled from the service mode.			
Y/C CRT Drive	A	Input = Component Video. Output = RGB. Adds Menu OSD from QM board.			

HD & Twin View Mode Video Troubleshooting

When there is a video problem in a high definition picture, you can use the twin picture mode and the built in video generator to isolate the problem to a board without removing the back panel. The Video Adjustment section of this book contains instructions on how to access the video generator from the service mode.

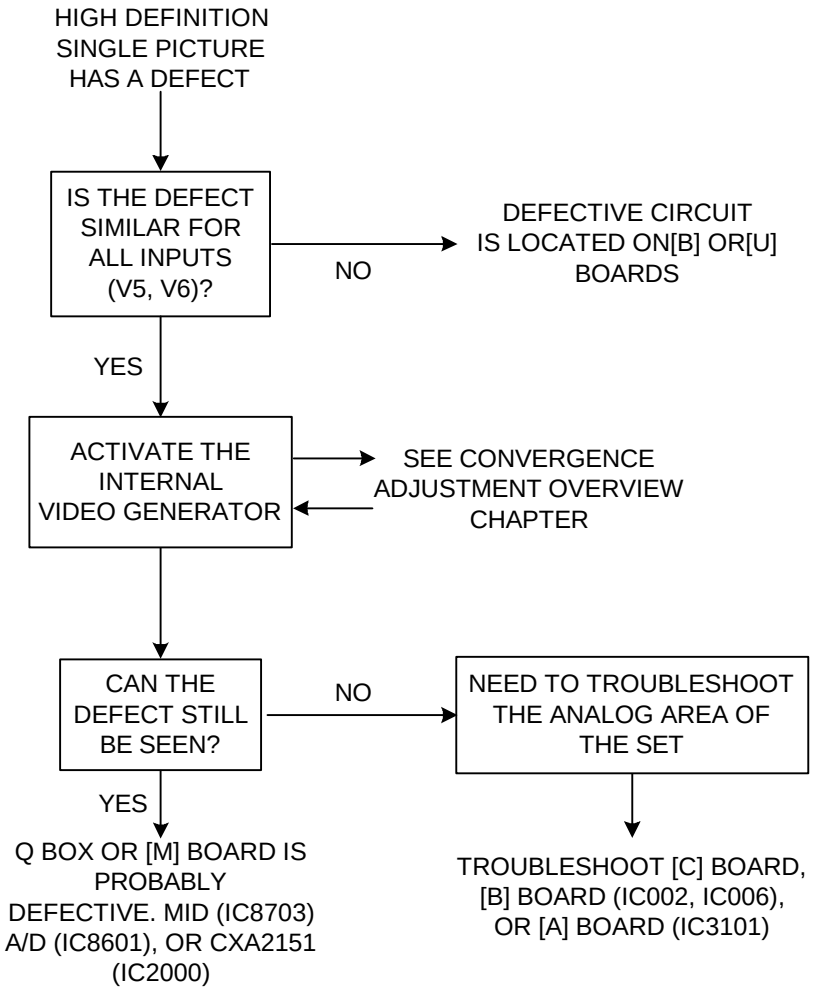

HIGH DEFINITION SINGLE PICTURE HAS A DEFECT
IS THE DEFECT SIMILAR FOR ALL INPUTS (V5, V6)?
NO
DEFECTIVE CIRCUIT IS LOCATED ON[B] OR[U] BOARDS
YES
ACTIVATE THE INTERNAL VIDEO GENERATOR
SEE CONVERGENCE ADJUSTMENT OVERVIEW CHAPTER
CAN THE DEFECT STILL BE SEEN?
NO
NEED TO TROUBLESHOOT THE ANALOG AREA OF THE SET
YES
Q BOX OR [M] BOARD IS PROBABLY DEFECTIVE. MID (IC8703) A/D (IC8601), OR CXA2151 (IC2000)
TROUBLESHOOT [C] BOARD, [B] BOARD (IC002, IC006), OR [A] BOARD (IC3101)

FIGURE 11-12 - FLOW CHART 3 - VIDEO TROUBLESHOOTING - ATSC SIGNAL 41TVP12 1356

Component Level Repair

Detailed Video Signal Flow

The video signal flow is divided into four parts as shown in Chart 11-7. A block diagram represents each part.

Chart 11-7 - HA-3 Video signal flow				
Figure #	Title	Board(s)	Input	Output
11-13	Video Process 1	A, U, HB, B	All NTSC inputs	Component Video
11-14	Video Process 2 - DTV Video	B, QM,	Component Video, EMI DTV bus	Component Video, Sync, Menu OSD.
11-15	Video Process 3	QM, B, A, C	Component Video, Sync, Menu OSD.	RGB to CRT cathodes
11-16	DTV Tuner	QM	UHF antenna / Memory Stick	EMI video bus, DTV line audio output

Video Process 1

The first Video Process (Figure 11-13) shows the composite and component video inputs to be NTSC processed on the B board. Chart 11-7 shows the signal flow and board input/output signal types.

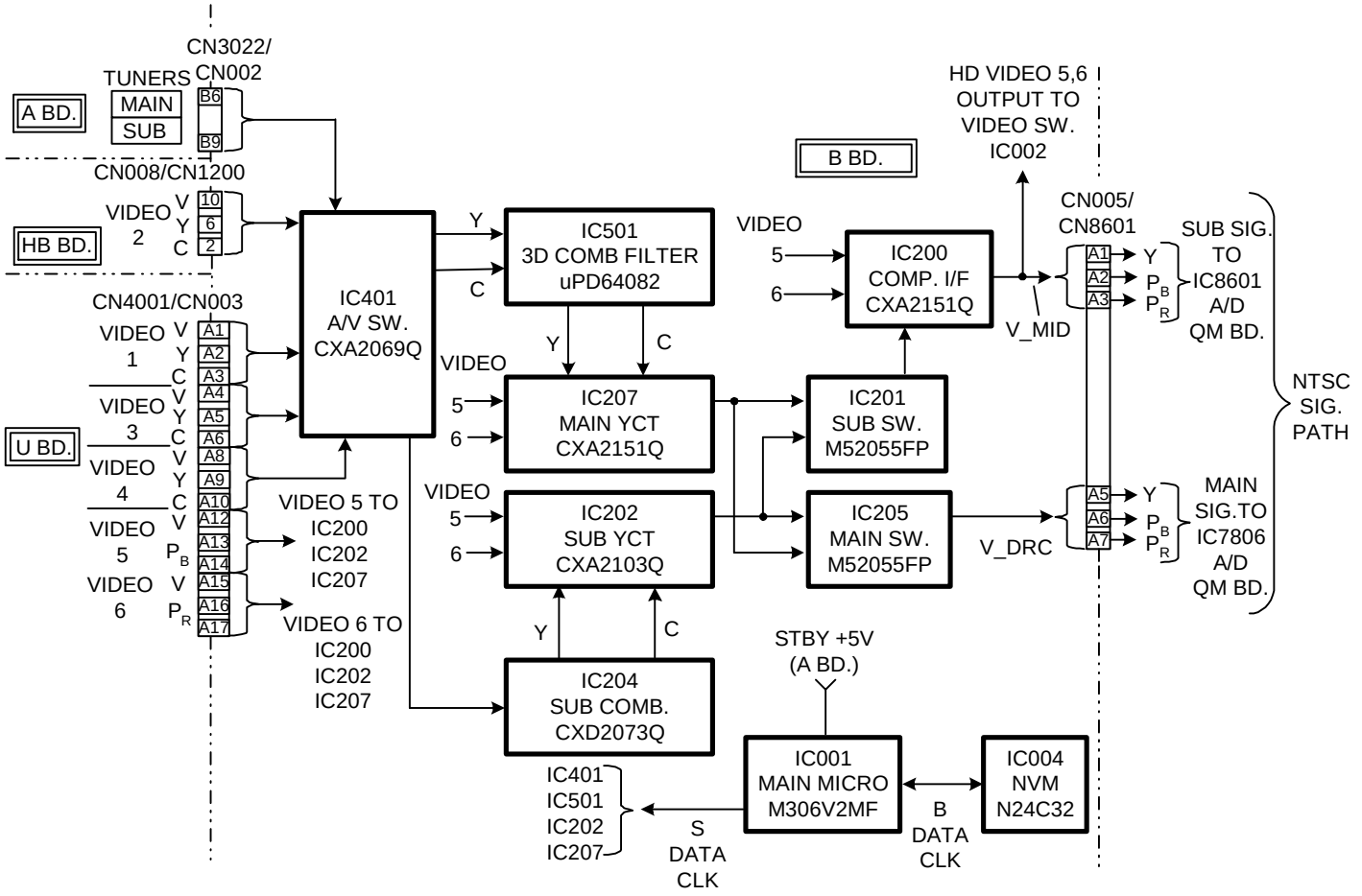


FIGURE 11-13 - VIDEO PROCESS 1

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Chart 11-8 shows the main and sub video signal flow through the B board.

Chart 11-8 – Video Process 1 Signal Flow				
IC	Name	Board	Function	Mode used
IC401	A/V Sw	B	Selects Main & Sub video inputs	When NTSC inputs are selected
Main Path				
IC501	3D Comb Filter	B	Separates the luminance form the chroma.	All NTSC modes except S video
IC207	Main Y/Ct	B	Selects input component video 5, 6, or composite video from IC501. Adds Closed Caption graphics	All NTSC modes
IC205	Main Sw	B	Swaps Twin View pictures back to original position	All NTSC modes
Sub Path				
IC204	Sub Comb Filter	B	Separates the luminance from the chroma.	Twin View
IC202	Sub Y/Ct	B	Selects input component video 5, 6, or composite video from IC501. Adds Closed Caption graphics	Twin View
IC201	Sub Sw	B	Swaps Twin View pictures back to original position	Twin View
IC200	Component Interface	B	Selects NTSC sub video or HD video 5, 6.	Twin View and HD video input

Video Process 2

The main and sub NTSC component video signals from the B board enter the QM board for processing as listed in Chart 11-9a. The signal flow is joined by the DTV tuner signal shown in Figure 11-15. All three signals flow into the MID IC8703 for selection.

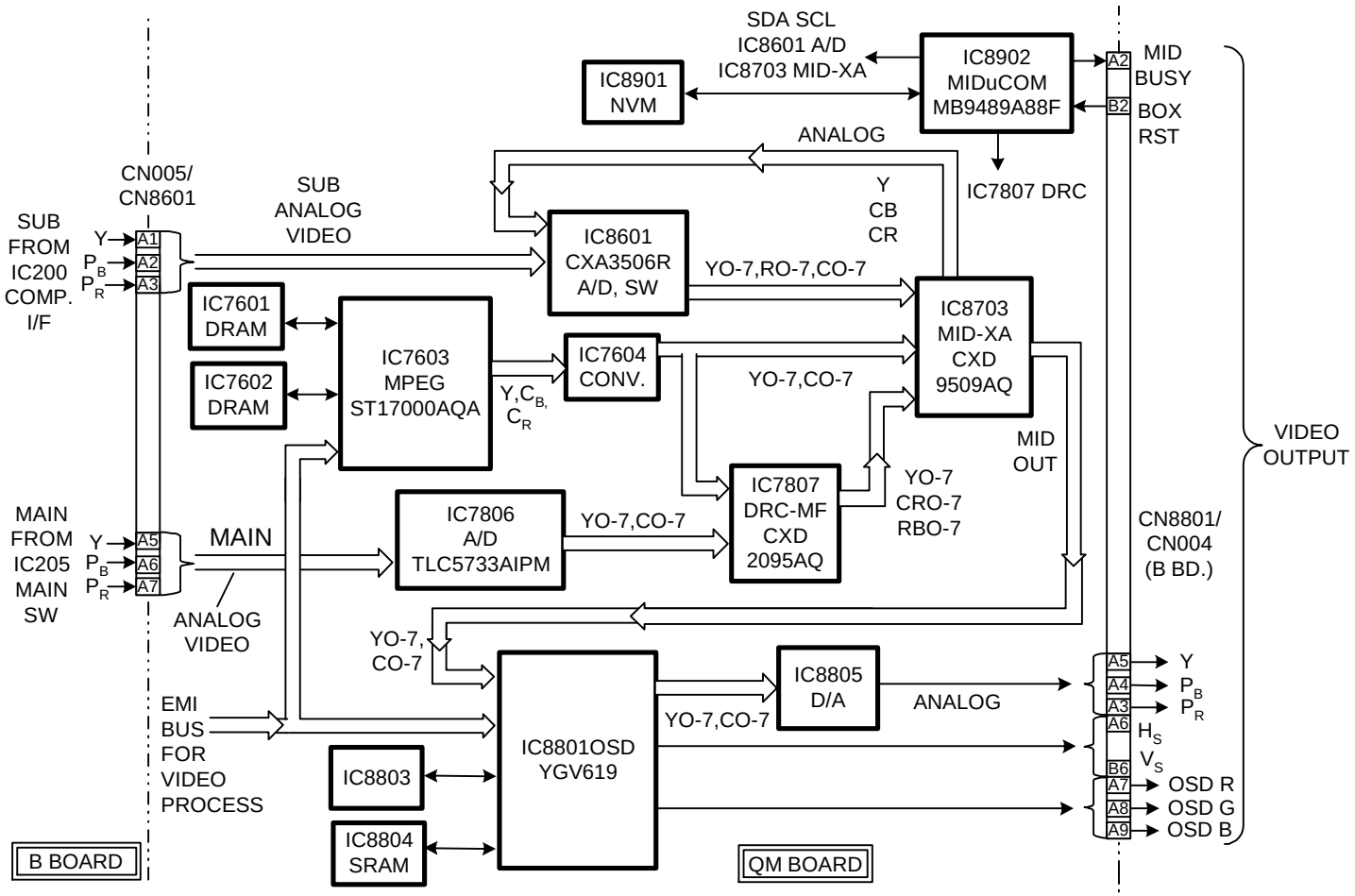
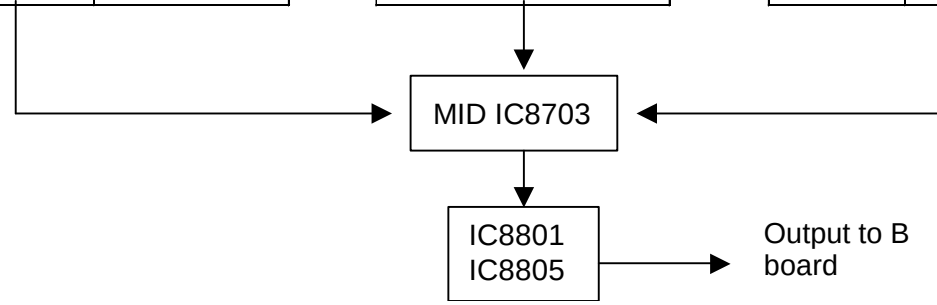


FIGURE 11-14 - VIDEO PROCESS 2 - DTV VIDEO 3TVP12 1320 9/6/01

Chart 11-9a - QM board Signal Processing								
Main Signal			DTV Signal Path			Sub Signal		
IC	IC Name	Purpose				IC	IC Name	Purpose
IC7806	A/D Conv	Digital Conversion	DTV Tuner			IC8601	A/D Conv	Digital Conversion
IC7807	DRC-MF	Increases pixel count	IC7205 to EMI bus					
			MPEG IC7603					



These three (Main, DTV and Sub) signals are input to MID IC8703. This MID IC will select either one input for normal TV operation or combine two inputs into a single picture for the Twin mode. The signal from MID IC8703 will continue into OSD IC8801.

Chart 11-9b - QM board Signal Processing (continued)		
IC – Signal Flow	IC Name	Purpose
IC8703	MID-XA (Multi Image Driver)	Twin View, H freq. conversion
IC8801	OSD	Buffer for video, Menu OSD
IC8805	D/A	Analog Conversion

Video Process 3

Refer to Figure 11-15 to follow the signal flow. The conversion of Component video to a high-resolution picture by the DRC and then being sized by the MID circuitry to fit on the screen is performed on the QM board. The component video output passes through the B board into the A board. The (white) menus OSD at CN004/pins A7-9 mix with the green OSD graphics (channel numbers, volume etc) from the main micro using Q9, Q11 and Q13. The combined OSD signal and buffered component video are applied to Y/C CRT Drive IC3101 on the A board. IC3101 mixes the video signal and OSD then converts the result into an RGB signal for the CRT on the C board.

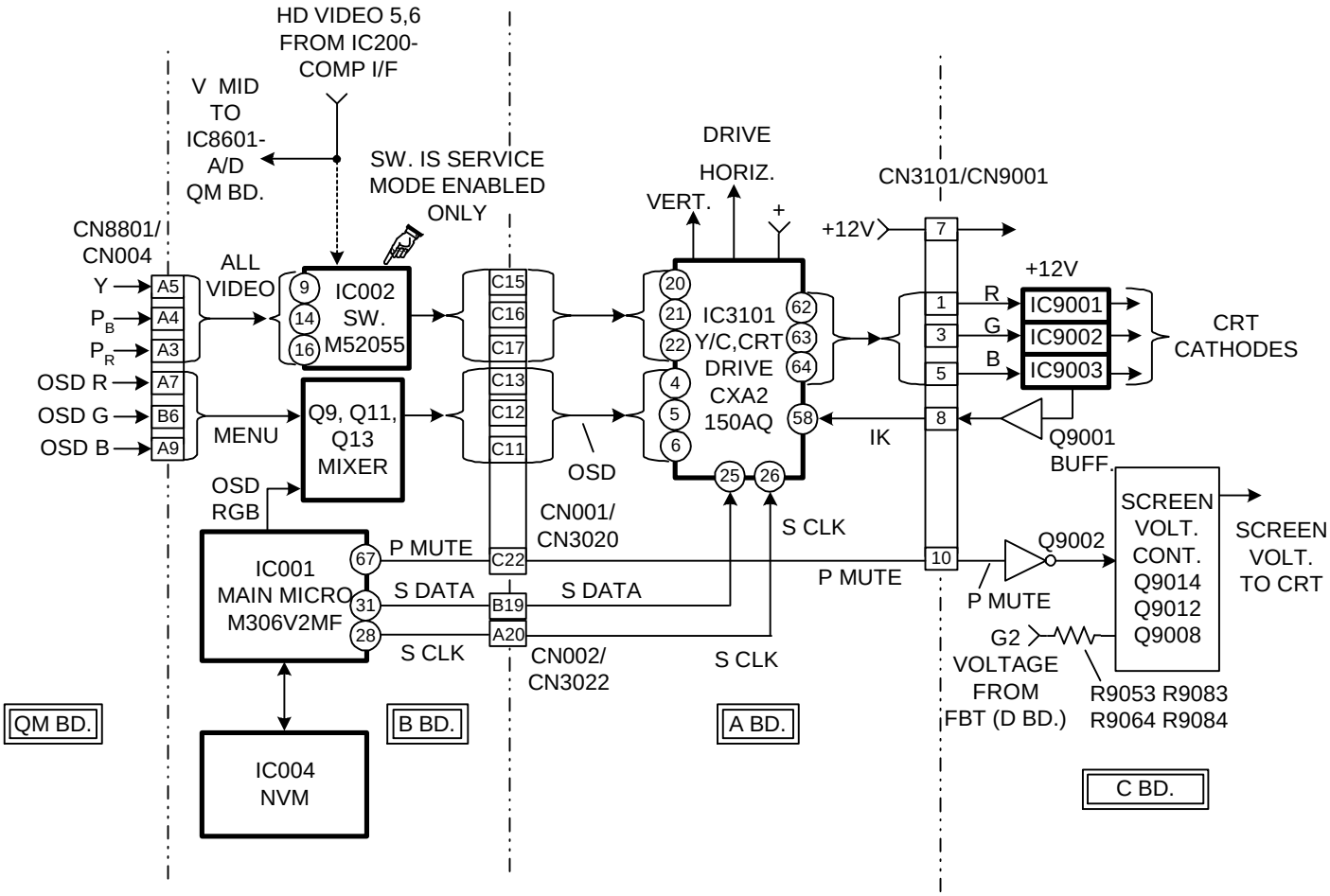


FIGURE 11-15 - VIDEO PROCESS 3

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DTV Tuner Processing for DTV Box Repair (HA-3 & RA-5A Chassis)

Refer to Figure 11-9 for the location of connectors and Figure 11-16 for the DTV tuner support signal diagram.

The DTV tuner needs various voltages for operation. They are easy to check at the Q box (CN7001). The DTV tuner receives the 8VSB modulation and delivers that signal to Digital microprocessor IC7205.

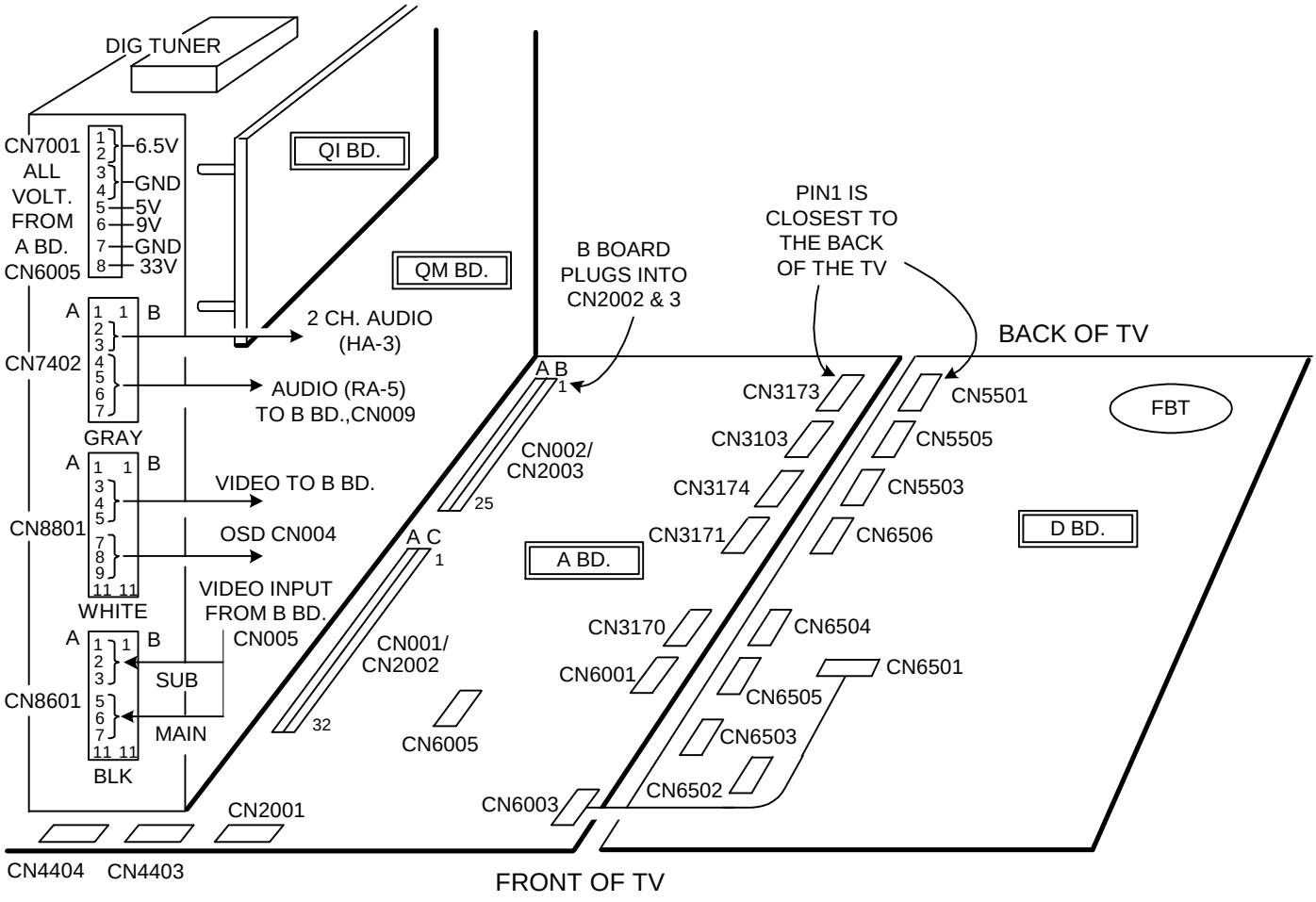

FIGURE 11-9 - HA-3 CHASSIS CONNECTOR LAYOUT 38TVP12 1354 9/4/01

IC7205 is one of three microprocessors in this TV that communicate with each other. Two are in the Q box and the Main Micro is on the B board.

Chart 11-10 –Microprocessor Responsibilities		
IC9209 MIPS CPU	IC7205 Digital Micro Processor	IC001 Main Micro
i Link operation	Memory Stick port access	Service mode & green user OSD
	DTV video & audio processing	TV Protection / Diagnostics
	DTV Tuner control	Power Supply Control
		NTSC tuner control
		Q box reset & Master communications

There are two LEDs inside the Q box near the DTV tuner. The green LED lights when a DTV station contains the 8VSB modulation scheme. The red error LED lights when the DTV signal stream does not contain the basic ATSC ID bits in the digital data (wrong data – not ATSC format).

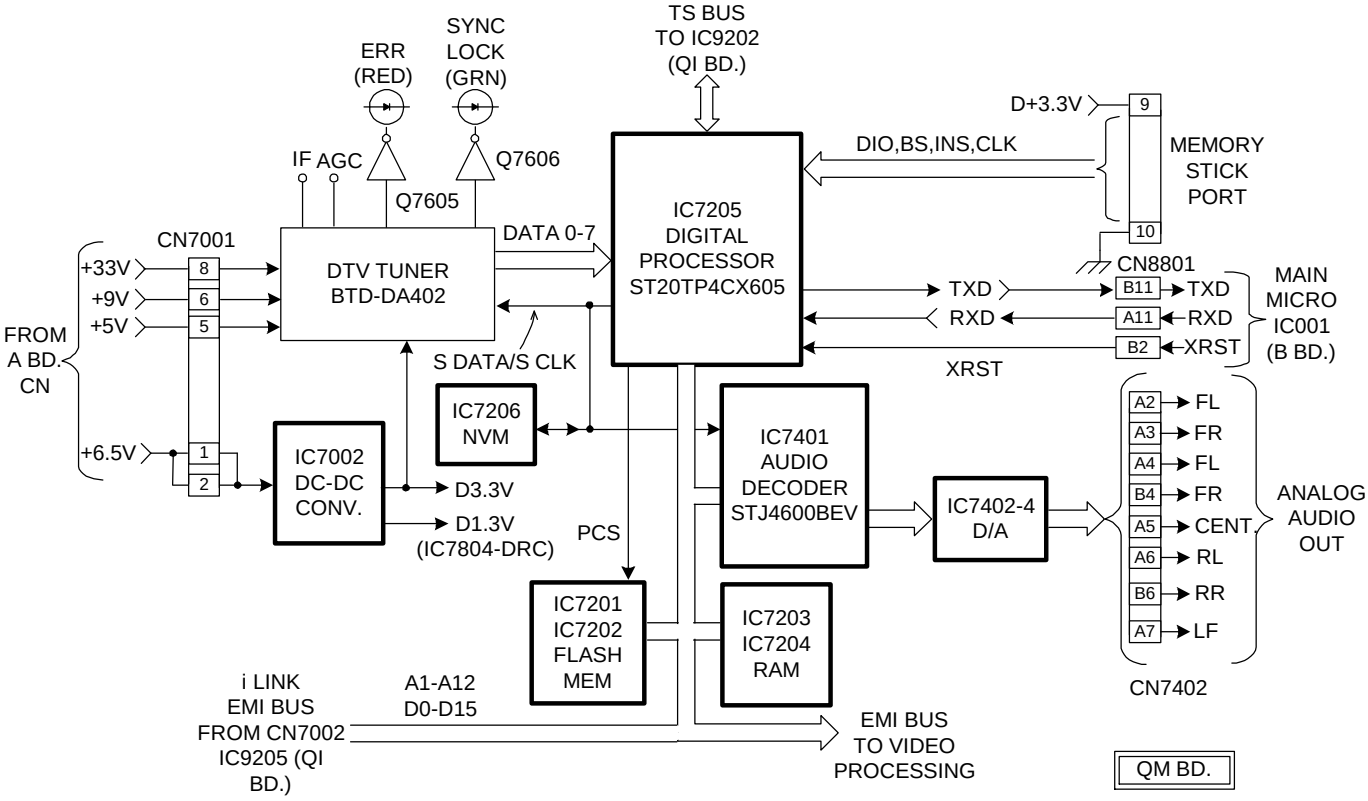

FIGURE 11-16 - DTV TUNER & AUDIO

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The EMI bus carries the DTV digital tuner data to the MID circuit for switching into the video path. See Figure 11-14 for the completion of the EMI bus.

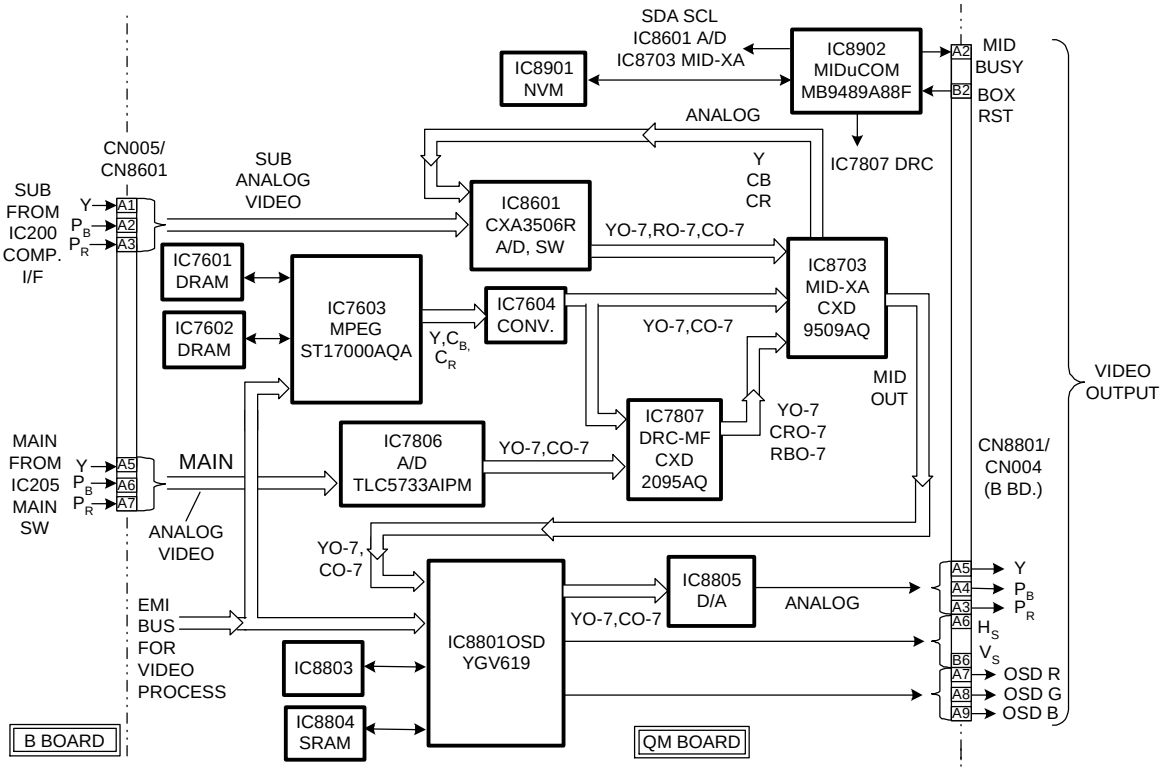

FIGURE 11-14 - VIDEO PROCESS 2 - DTV VIDEO

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Audio Block (HA-3 Chassis)

Refer to the audio block Figure 12-1 for the description and board flow of the audio processing.

Signal Flow

- The audio input signal hops from the B board to the S, and finally to the A where the output amplifiers are located. The audio can either output the internal speakers or the rear panel phono jacks when the speakers are turned OFF (from the menu).

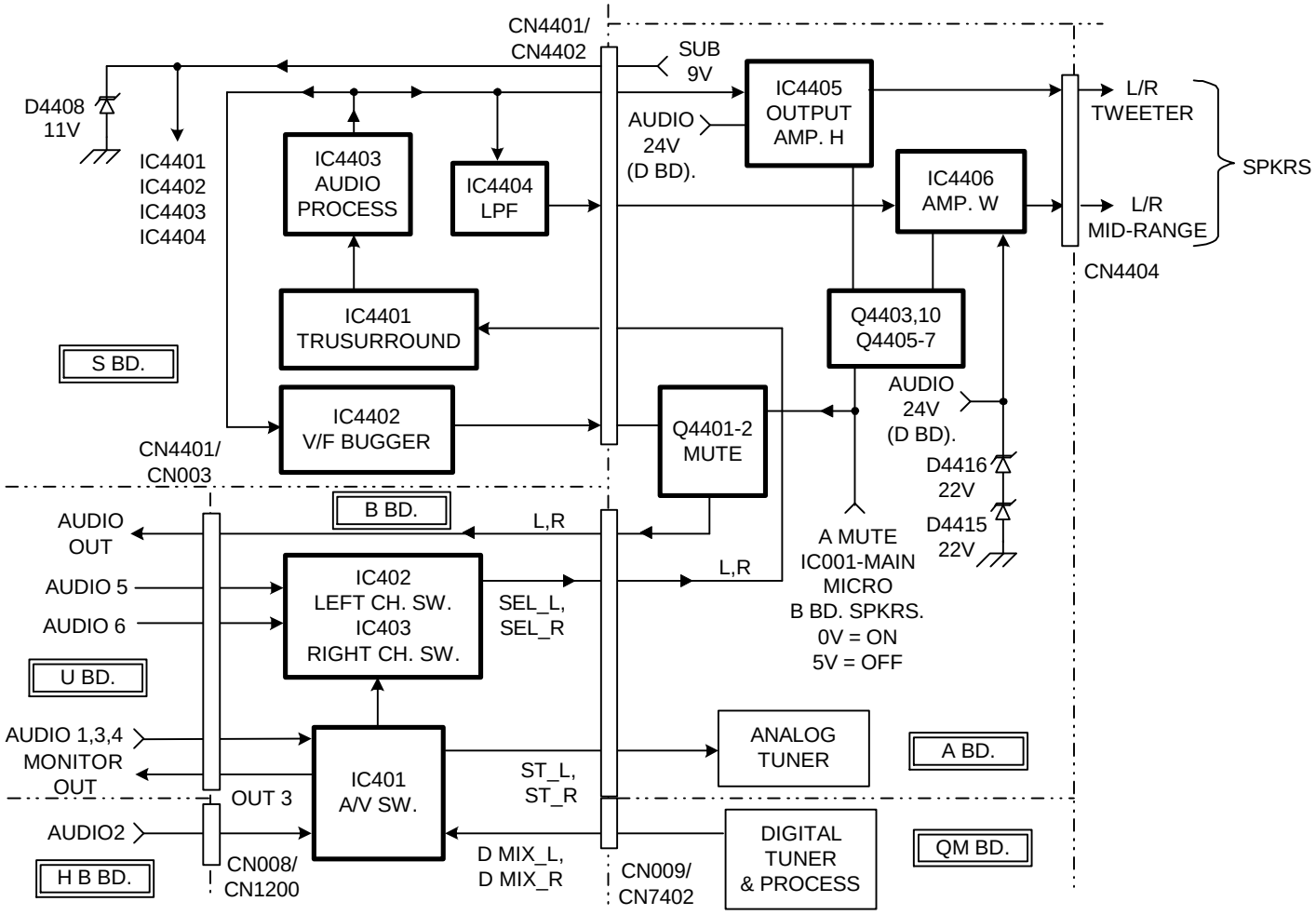

FIGURE 12-1 - AUDIO BLOCK - HA-3 CHASSIS

B Board

There are three audio sources input to the B board:

- Analog TV tuners
- Video / audio jacks
- Digital tuner

On the B board, a single selection is made and both Sel_L and Sel_R audio channels pass through the A board for processing within the S board.

S Board

Chart 12-1 shows the functions of all four ICs on the S board.

Chart 12-1 - S Board ICs		
IC / Name	Mode used	Purpose
IC4401 / TruSurround	When TruSurround is selected from the "Effects" menu.	Produces the surround sound illusion when stereo sound is input. S Mode from Main Micro IC001/pin 88 (CN4401/pin 6) goes HIGH to turn on Surround Sound.
IC4403 / Audio Process	All modes	Controlled by serial data from Main Micro IC001 (B board – not shown) Sets Volume, Tone, Balance, & Simulated Mode (echo effect for mono signals).
IC4404 / Low Pass Filter	Speakers ON	Passes only the low frequencies to the internal midrange spk.
IC4402 / Variable/Fixed Audio Buffer	When speakers are switched OFF	Rear panel audio output jacks can be used to feed an external Dolby 5.1 channel or DTS amp or headphones.

IC4401 TruSurround

Both Sel_L and Sel_R audio signals enter the S board and are applied to IC4401. IC4401 either passes the audio out of the IC or creates a 3D sound field when the TruSurround mode is activated from the menu. When activated, Main Micro IC001 outputs a HIGH at the "S Mode" line that can be checked at the S board (CN4401/pin 6). Chart 12-2 shows IC4401's control voltage.

Chart 12-2 - TruSurround IC4401 Control Voltage		
Audio Effect	Location	Voltage
Off	CN4401/pin 6	0Vdc (OFF)
Simulated	CN4401/pin 6	0Vdc (OFF)
TruSurround	CN4401/pin 6	5Vdc (ON)

IC4403 Audio Process

Audio Process IC4403 controls all other audio effects from volume, tone, balance, to echo effects used in the menu's Simulated Audio Mode and BBE Mode (RA-5A chassis only). IC4403 output takes two paths. The main path leaves the S board as the High output. The second path goes into a Low Pass Filter IC4404 to remove the high frequencies before leaving the board as the woofer output.

A Board

Two power amplifier ICs are fed by a zener protected 24Vdc source. One power amp processes both channels of the high frequency signal and the other processes the low frequency signal from the low pass filter. The power amplifiers can be muted when speakers are turned OFF from the menu. When the speakers are turned OFF, the variable or fixed line output is enabled.

Normal Signal Levels

Refer to chart 12-3 for the audio signal levels throughout the audio chain. The audio signal is taken from a B&K 1064 NTSC pattern generator with 1kHz audio modulation input to the sub tuner's channel 3. The DTV audio level is the average volume sampled from four DTV stations.

Chart 12-3 - Audio Signal Levels			
	Test Location		
Signal	Left	Right	Level *
DTV Output	CN7402/pin A2 (QM board)	CN7402/pin A3	0.4Vp-p (average)
Analog Tuner	Main or Sub Tuner pins (A board)	Main or Sub Tuner pins (A board)	1.4Vp-p (1kHz)
B Board Output	CN4401/pin 8 (S board)	CN4401/pin 9 (S board)	1.4Vp-p w 5Vdc
Mid & Tweeter out to Amp **	CN4401/pin 1 (S board)	CN4401/pin 2 (S board)	0.1Vp-p at half volume ** 0.6Vp-p = Max volume
Low freq Output to Amp	CN4401/pin 3 (S board)	CN4401/pin 4 (S board)	0.018Vp-p = half volume, 0.03Vp-p = Max volume
Variable / Fixed Output ***	CN4401/pin 11 (S board)	CN4401/pin 12 (S board)	0.22Vp-p = half volume, 2.0Vp-p = Max volume 1.5Vp-p = Fixed output

* All effects are turned OFF from the menu.

** Output level at half volume changes to 90mVp-p in Simulated Mode or 120mVp-p in TruSurround Mode.

*** Main Micro IC001 Mute control line "A Mute" at CN001/pin A1 either selects speakers (HIGH) or the rear panel variable / fixed audio output (LOW).

Firmware Upgrade

Each HA-3 direct view and RA-5A projection TV chassis contains a built-in DTV decoder. Although the main DTV format is set by the ATSC standard for the US and Canada, changes to the fine DTV transmission will take place as the format details are ironed out. To maintain future compatibility in the face of changing standards, the DTV's flash memory can be upgraded (replaced) with data from a plug-in memory stick.

Upgrade Procedure:

The upgrade requires the technician to insert the memory stick when the TV is OFF. The TV must then be turned ON to recognize the memory stick and begin the upgrade. The upgrade status LED (TV rear panel above the memory stick port) begins flashing while the TV's OSD displays "Memory Upgrade Mode" on the screen. When the screen goes dark, the upgrade is in progress. All the TV user functions are inhibited until the upgrade is finished. At the end, the upgrade status LED changes the blink rate to indicate a successful or unsuccessful upgrade completion. It flashes quickly for success or stays ON for one second. When unsuccessful, it stays OFF for two seconds while flickering. The memory stick must be removed to resume TV operation or left inserted for another attempt.

Technical Upgrade Operation

Refer to Figure 13-1 for the technical operation.

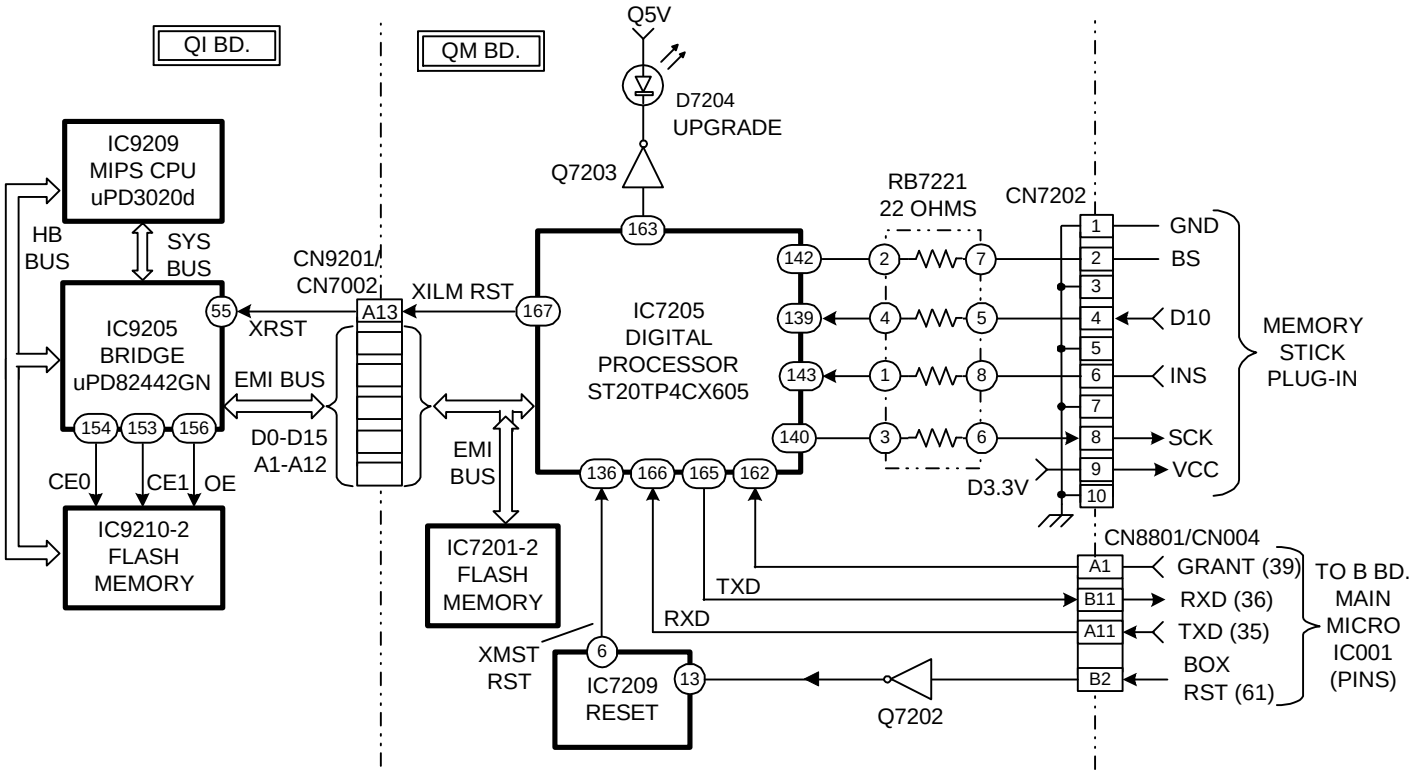

FIGURE 13-1 - MEMORY STICK UPGRADE CIRCUIT

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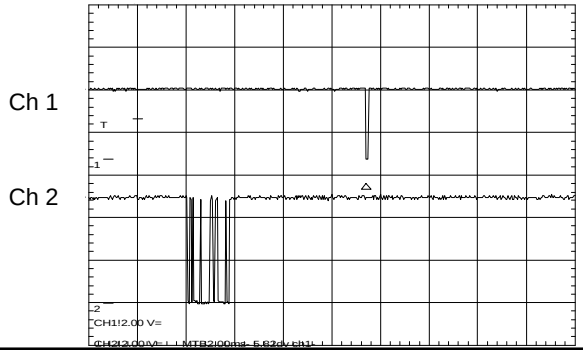
1. The upgrade memory stick must contain two files and supporting data. Insert the Memory Stick into CN7202 (QM Bd) to begin the upgrade. The memory stick brings the INSERT line at CN7202/pin 6 LOW.
2. IC7205 responds by flashing the D7204 LED.

3. IC7205 (QM Bd) uses TXD and RXD to communicate with Main Micro IC001 (B Bd). When IC7205 requests a memory upgrade operation, IC001 must interrupt the normal TV operation.
   Waveform 13-1 shows typical Q box to Main Micro IC001 (B Bd) bi-directional communications. Normally there is only periodic communications and then only when needed. This waveform was taken when changing into a DTV station (channel up command). In the waveform sequence, notice that the Main Micro starts the communications (ch 2) and the Q board micro replies afterwards (ch 1). When changing into NTSC stations that do not require the Q box to select a station, there is no (ch 1) reply. Note that the output of the Q box is 5Vp-p and the reply signal from IC001 is only 3Vp-p.



Waveform 13-1 – Microprocessor Communications* QM – B Board

Channel	Signal Name	Location	Vp-p
1	RXD to Main Micro IC001 (B Bd)	CN8801/pin B11	3Vp-p
2	TXD	CN8801/pin A11	5Vp-p
Time Base = 2msec/div.			
* Taken when channel changing into a DTV station. When changing to another NTSC station, RXD signal (ch 1) from the Q box is not present.			

4. Main Micro IC001 displays “Memory Upgrade Mode” on the screen.
5. Main Micro IC001 then blanks the screen and outputs a Grant and reset (XRST) line to begin the upgrade. After resetting the Q box microprocessors, IC7205 and IC9209, the upgrade sequence starts.

Chart 13-2 - IC001 Outputs to Q board to begin Memory Upgrade		
IC001 Output	Location	Voltage
Grant	CN8801/pin A1 (QM Bd)	HIGH
XRST	CN7201/pin A2 (QM Bd)	Momentary LOW

6. IC7205 checks for the first folder of data and if present, loads these files into the two Flash Memories (IC7201-2) on the QM board.
7. Next IC7205 checks the memory stick for the second folder. When found, IC7205 instructs MIPS CPU IC9209 to complete the loading process.
8. MIPS CPU IC9209 loads the second folder into two flash memories (IC9210-1) on the QI board via IC9205. Bridge IC9205 serves as an interface IC between the EMI and HB bus completing the communications path.
9. When finished, MIPS CPU IC9209 sends an OK to IC7205 using bridge IC9205 and the EMI bus.
10. IC7205 pulses LED D7204 in a pattern to indicate success or failure. **If failure, the cycle repeats as long as the memory stick is inserted**.
11. Removing the memory stick permits IC7205 to inform Main Micro IC001 of the successful upgrade.
12. To return to normal TV operation, IC001 outputs a XRST momentary LOW to restart the Q box but this time the Grant line is kept LOW for normal operation. This is listed in Chart 13-3.

Chart 13-3 - IC001 Outputs to Reboot		
IC001 Output	Location	Voltage
Grant	CN8801/pin A1 (QM Bd)	LOW (no upgrade)
XRST	CN8801/pin B2 (QM Bd)	Momentary LOW

13. IC7205 informs IC001 the boot up is complete.
14. IC001 unblanks the CRT resuming normal TV operation.

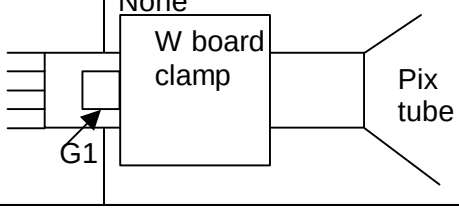
Upgrade error

IC7205 pulses the rear panel LED D7204 to show an error code if:

- IC7205 discovers there is no first folder on the memory stick.
- After loading the first folder, IC7205 discovers there is no second folder for IC9209 to upgrade.
- Memory stick is not making good contact.

HA-3 TV Chassis Board Replacement

Board	Circuits	Fuses		Zeners		After board Replacement
		#	Load	#	Purpose	
A	Standby Power Supply Degaussing circuit Primary Power Supply (9V, 5V, 3.3V) H & V Oscillators/Jungle Both Tuners Audio output	R6002	Primary PS	D4415, D4416	+24V OVP Audio Out B+	No Adjustments
				D6017	6.8V for pwr OFF A mute	
				D6015,20	Q6.5V OVP	
B	Video processing and audio switching. Closed caption/V Chip Main Micro IC001 OSD (Menu)	None		None		Transplant memory IC004 containing system and user data, including analog tuner active stations. ** see note below.
C	RGB CRT signal amplifiers	None		D9010	G1 Volt limiter	Adj Screen control according to the service manual: Reduce vertical size to see IK line at the top. Blank pix in the service mode* by changing CXA2150P-2/ALBLK data from 0 to 1. Adjust screen control so the IK line is just invisible in a dark room. Adj H Static Control

Board	Circuits	Fuses		Zeners		After board Replacement
		#	Load	#	Purpose	
D	Secondary Power Supply (+200V, +135V) Protection latch circuit HV Regulator circuit Corner focus circuit Top/bottom pincushion circuit H Output / V Output	R6236	Sec PS	D6508=33V	Reg Tuner voltage	Transplant memory IC5501 containing deflection parameters. Adj Focus (on FBT). Enter the service mode* and perform touch up geometry adjustments to D-Conv/CXA8070, CXA2150**D**-1 and CXA2026 data. Adjust HV RV8002 for 31.5kV. Adjust HV shutdown RV8001 according to safety related adj. in the service manual.
		PS6501, PS6502	24V Audio Output	D6025=33V D8006=13V	HV limit	
		R8051	Hi Volt PS			
		R5096	200V Video Output	D6004=5V	HV Protect ref	
				D5031=17V	Fbk pulse limiter	
		R5097-8	H Centering			
		R5099	Filament			
		R5576	DQP Amp (corner focus)	D5004=12V	MOSFET Protect	
		R5711 R5712	Conv Yoke Amp	D5007	DQP mute at pwr ON	
F	AV loss detection circuit Degaussing relay	F6701-	Main AC – 6A	None		No adjustments.
Q Box (Qi, QM Bds)	DRC for line doubling MID for twin pictures DTV Tuner and video processing	None		D7803	3.9V Reg for IC7805 (Write PLL) QM Bd.	No adjustments. Enter the service mode and verify the TV ID (group #19). ** see note below
S	Audio Processing	None		D4408-11V	Sub 9V line OVP	No adjustments.
				D4401-2 = 10V	line input protection	
U	Rear panel input/output connectors.	None		None		No adjustments.
W	Velocity Modulation circuit to improve detail. Top/bottom Pincushion and corner focus coils.	None		None		No adjustments. Note position of coils on CRT neck before removing the old board or corner distortion will occur.

* Enter the service mode from the remote control buttons: Display, Ch 5, Vol +, Power. See the Convergence Adjustment Overview chapter for more information about the service mode.

** After replacing the B board or Q box you will find that the plugs to CN8801 and CN8601 are the same. Cables from Q box to CN004 and CN005 should cross. See Figure 14-1.

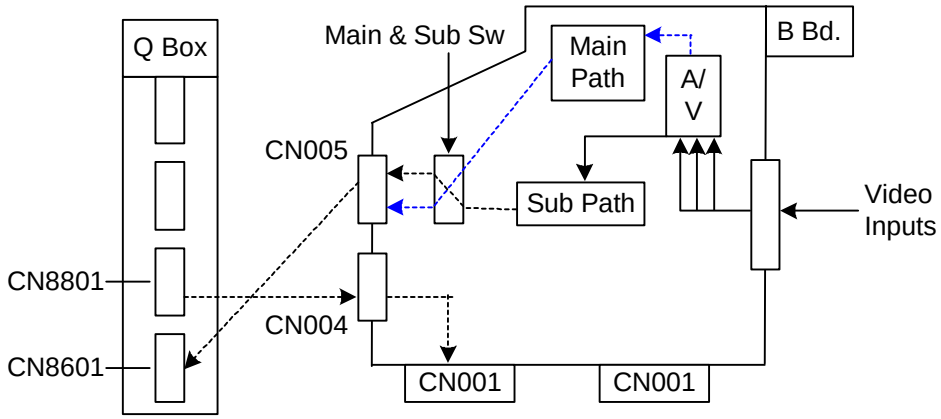


Figure 14-1 - HA-3 & RA-5A Video Path

NVM Contents

TV's Non Volatile Memory (NVM) Contents		
B board IC004	D board IC5501	QM board IC7206 and IC8901
Active Analog & **Digital** TV stations & last channel/video	Deflection parameters (raster parameters not video)	Picture parameters such as size, position, etc (video parameters not raster)
User Picture / Audio settings	CRT Drive settings	Single and Twin pix parameters
User Operation settings (DRC)		Freeze pix settings
Close caption		
Service mode model ID		

Convergence Adjustment Overview – HA-3 Chassis

HA-3 Adjustments are performed after CRT, D board or EEPROM replacement. The details are explained in the service manual. With so many details, the technician needs to get an overview of the adjustments so he can determine what he may see if his adjustment affects others. Generally, because the horizontal TV frequency is fixed at 33.5kHz for all four picture modes, there are less picture size and geometry adjustments than other HDTVs. Often, copying the main Full Mode data to the other modes is all that is required without touch up.

Service Mode Access (conventional)

In Standby (power OFF), point the remote to the TV and press the following four buttons in sequence:

Display, 5, Volume + and Power On.

Service Mode Categories (Groups)

There are so many service mode adjustments possible that they are grouped into "categories". Within the category are "items" that you can adjust. Finally changing the "data" for the item will make the adjustment. See Figure 15-1 below:

FIGURE 15-1

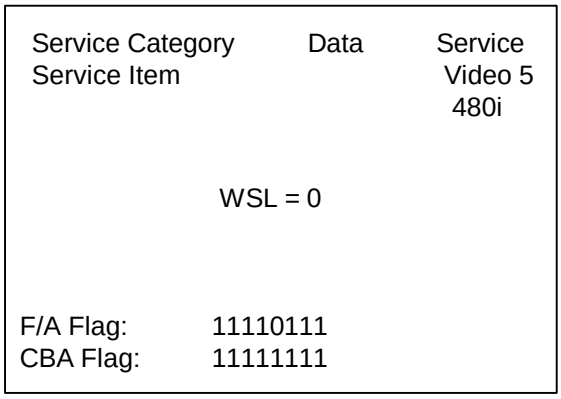


Chart 15-1 on the next page summarizes the service mode categories for the HA-3 TV chassis. The RA-5A chassis has an additional PJE category for convergence. Use the 2 (up) or 5 (down) remote buttons to change categories in the service mode. This chart permits you to get to the category faster and prevents you from missing the category. Locate the category you are at on the chart and then determine where you want to go. You can then take the shortest path (up or down) to get there.

Chart 15-1 - HA-3 Chassis Service Mode Categories			
Category	NVM Data Location (Board)	Purpose	Copy Function ?
Version	Q Box	Versions of ICs in box	
3D-Comb	B	Y/C separation parameters	
2103 (1-2)	B	NTSC pix parameters	
2150P (1-4)	D	CRT Drive settings	
2150D (1-3)	D	Deflection parameters	Yes
D-CONV	D	Corner Convergence	Yes
CXA2026	D	Focus, Corner Conv.	Yes
CXA2151	B	NTSC Sync, YUV* gain	
MID (1-5)	Q Box	Video (pix) parameters	
CXA3506R	Q Box	Contrast settings	
BH3868	B	Audio settings	
TDA7312F,R,C	B	Audio settings	
SNNR	D	Noise reduction	
CCD	B	Close Cap parameter	
DTV	Q Box	Signal Info, test pattern	
TP	Q Box	Modl, Dmy1 ?	
OP	B	Main Micro Version, OSD position	
ID	B	Model /Feature Codes	

* YUV = Component Video (Y, Pb, Pr or Y, Cb, Cr)

Convergence Adjustments - Overview

These adjustments are found in the 2150D (1-3), D-CONV, and CXA2026 catagories of the service mode. They should be performed in the sequence given (by following the stepped procedure in the service manual). In other words, place the TV in the FULL picture mode form the menu and perform the adjustments starting with “H Centering” and finishing with “Outer vertical bow”. Next, switch to the NORMAL picture mode using the menu and perform “Vertical Pin” and so on. Do not perform the High Definition 1080i Mode adjustments first and then the Full Mode adjustments. Always check the Full, Normal, Zoom, Wide Zoom and finally the High Definition 1080i Modes while adjusting in that order.

Full Mode

1. H Center
2. V Position
3. V Size
4. H Position
5. H Size
6. V Centering
7. V Pin
8. H Keystone
9. Vert Linearity
10. S Correction
11. H Linearity
12. H Middle Pincushion
13. H. Outer Pincushion
14. Top and Bottom Pincushion
15. Vertical Keystone
16. Left and Right Vertical Slant (Angle)
17 . Overall Vertical Slant
18. Vertical Bow
19. Outer vertical Bow

Normal Mode

Vertical Pincushion

Zoom Mode

1. Vertical Size
2. Vertical Position

Wide Zoom Mode

1. Vertical Center (Video)
2. Vertical Size
3. Horizontal Outer Pincushion
4. Horizontal corner Pincushion
5. Vertical Keystone

High Definition 1080i Mode

1. Vertical Size
2. Vertical Position (Video)
3. Horizontal Position (Video)

Data Copy Function

The copy operation is only found in the service mode categories that contain convergence data. See Chart 15-1. The purpose of the copy function is to copy the data within that category from the Full Mode to the other display modes such as Normal and Zoom. The data should be the same in this TV because the deflection has not changed in these other modes (horizontal frequency is always 33.75kHz in all picture modes). The different modes are accomplished by changing the video signal.

Procedure

1. Perform convergence or geometry adjustments in the FULL Picture Mode.
2. When you finish making adjustments to that category, use buttons 1 and 4 on the remote to go to the “CPY” item in that category (CPY 1, CPY 2 or CPY 3 is the last item in the category).
3. While on the CPY item, Change its data from 0 to 1 (button 3).
4. Press the Mute button.
5. Press the Enter button.

The data from the Full mode in the category you are in is copied to the remaining picture modes.

Internal Video Pattern Generation

The Q boards can generate patterns in 1080i, 720p, 480p and 480i when receiving a DTV station.

1. Enter the service mode.
2. Go to a DTV station or input a 1080i video input, otherwise the patterns will not be displayed.
3. Select category “DTV” (buttons 2 and 5).
4. Select item #1 (PATN) using buttons 1 or 4. You can select 1080i, 480 or 720p video patterns by choosing the data numbers 1-39 (buttons 3 and 6) as shown in Chart 15-2.

Chart 15-2 - Generator Patterns				
Pattern	Data # for 1080i pattern	Data # for 480i pattern	Data # for 480p pattern	Data # for 720p pattern
Black screen	0	16	26	36
Cent Hatch	1	11	21	31
Color Bars/B-W	2	12	22	32
White Square	3	13	23	33
Color Bars	4	14	24	34
White	5	15	25	35, 37,40
Black	6	16	26	36
Gray scale	7	17	27	
Low to High Freq Sweep	8	18	28	38
Gray	9	19	29	39
Diamond	10	20	30	

The video patterns are generated on the QM board taking the following path to OSD IC8801 in Chart 15-3.

Chart 15-3 - Video Pattern Generation			
IC	Bd	Name	Purpose
IC7205 / ST20TP4CX604	QM	Dig Process	Stores the pieces of the video pattern
IC7203,4 / GM71VS65163	QM	D RAM	Lays out the pieces (map)
IC7603 / STI7000AQA	QM	MPEG Decoder	Inserts the map into the video chain
IC8801 / YGV619	QM	OSD	Pass-through out of the bd.

Alternate Video 5/6 input Path – used for troubleshooting only

(Q box video bypass is NOT fully tested)

Purpose

All video must pass through the Q box, including TV. When the Q box video path operation is in question, HD 1080i video 5 or 6 input can be routed in a direct path to the CRT if the service mode is operational.

Alternate Signal Path

This alternate path is from the input, B board, A board and C board to the CRT for a normal picture. Refer to Figure 15-2 and see the Video Processing for details of the alternate signal path.

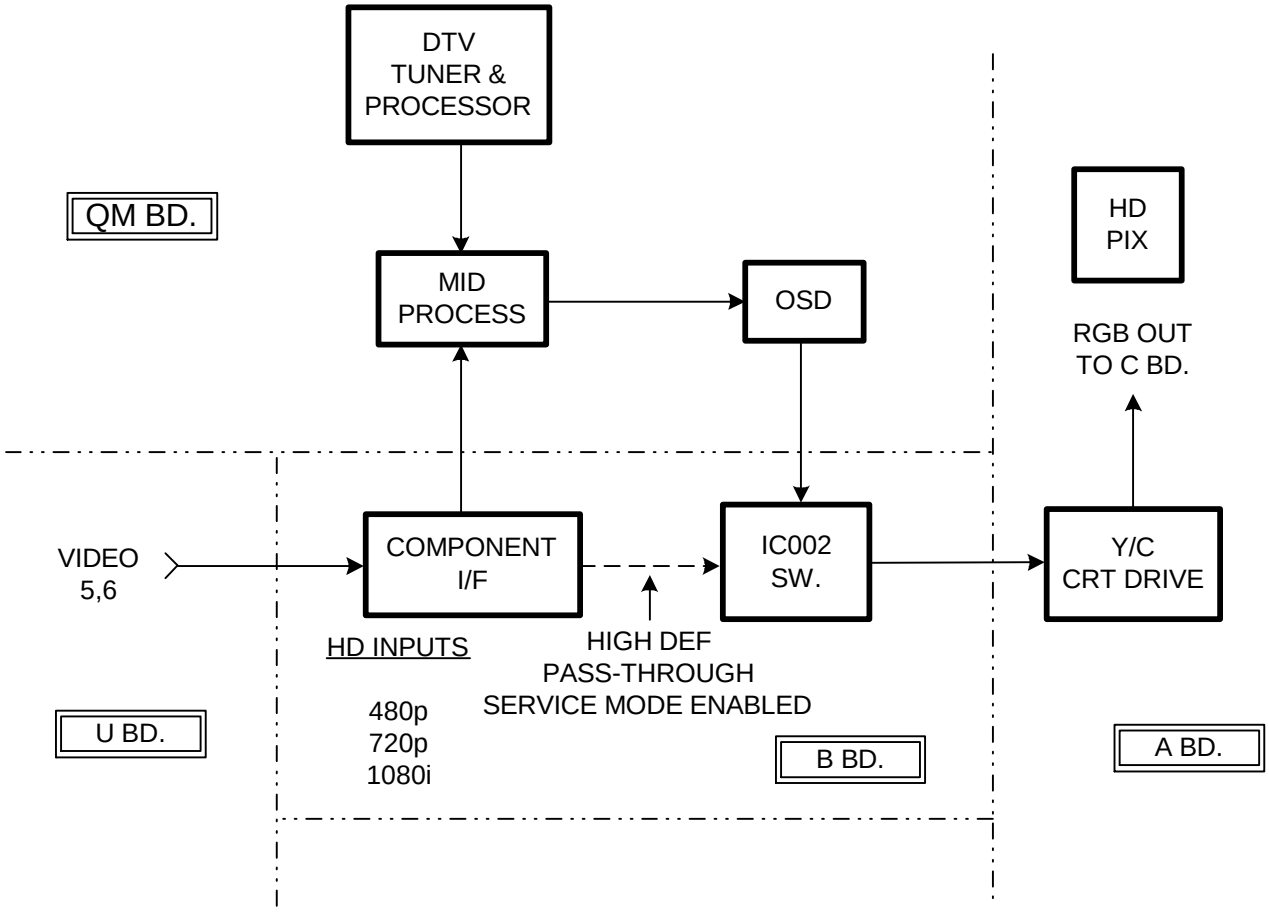


FIGURE 15-2 - HD VIDEO PATH 10TVP12 1328 8/31/01

Procedure

Rerouting the HD video path is done from the service mode. The Q board must remain connected (CN8801 for communications and CN7001 for power) for you to see the servicing mode OSD to make the change.

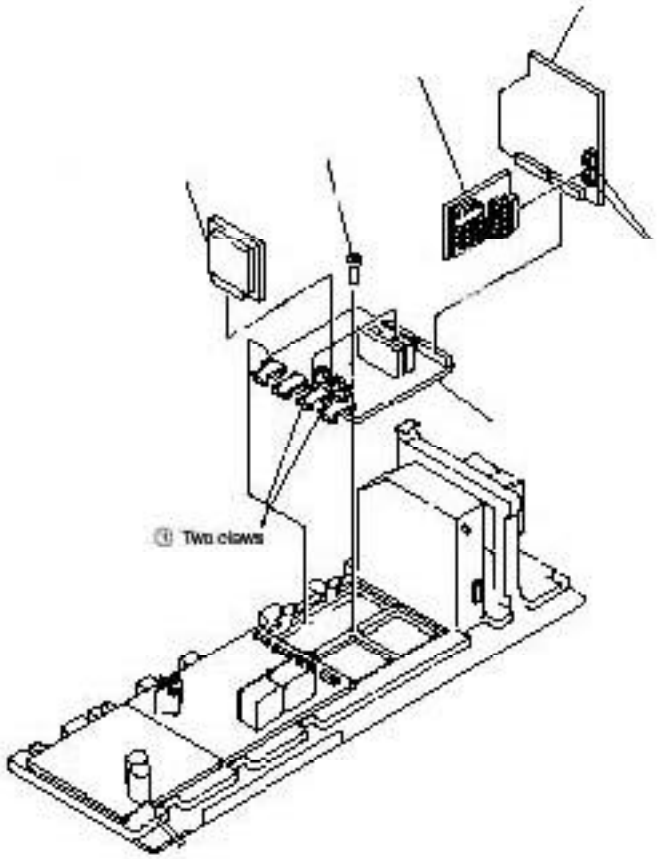
1. Enter the service mode (Display, 5, Volume +, Power On).
2. Select category “OP” (buttons 2 and 5).
3. Select item “HDPT” (buttons 1 and 4) (HDPT means High Definition Pass Through, item 5).
4. Change its data from 0 to 1.

Only a 1080i video input signal will display a picture because it solely has a 33.75kHz signal frequency that matches the TV’s horizontal frequency of this Hi-Scan TV. All the other signal inputs must be converted by the MID circuitry within the Q box (Q boards) to view. Chart 15-4 shows the horizontal frequency of the DTV formats at the popular 60Hz Vertical frequency.

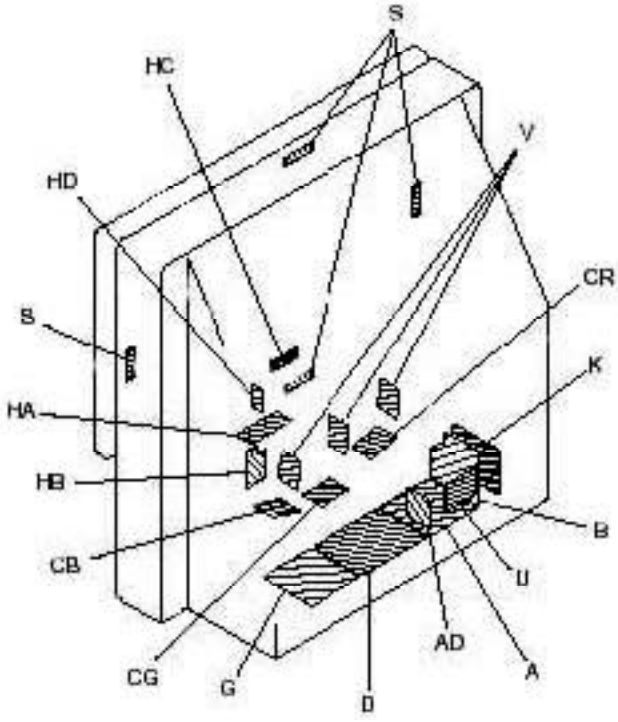
Chart 15-4 – Input signal H. Frequency	
Input signal	Horizontal Frequency
Standard NTSC 480i	15,734 Hz
High Resolution 480p	31.5kHz
High Resolution 720p	45.kHz
High Resolution 1080i	33.75kHz

RA-5A Chassis Board Layout

AD, U, B, AND A BOARDS REMOVAL



CIRCUIT BOARDS LOCATION



RA-5A Chassis Overall Block

The HA-3 Direct View TV Chassis and the RA-5A Projection TV chassis share almost identical B and Q boards (except for software), making the video processing flow the same. The two sets differ in the location of power supply and convergence stages. Refer to Figure 17-1 for the descriptions of these stages.

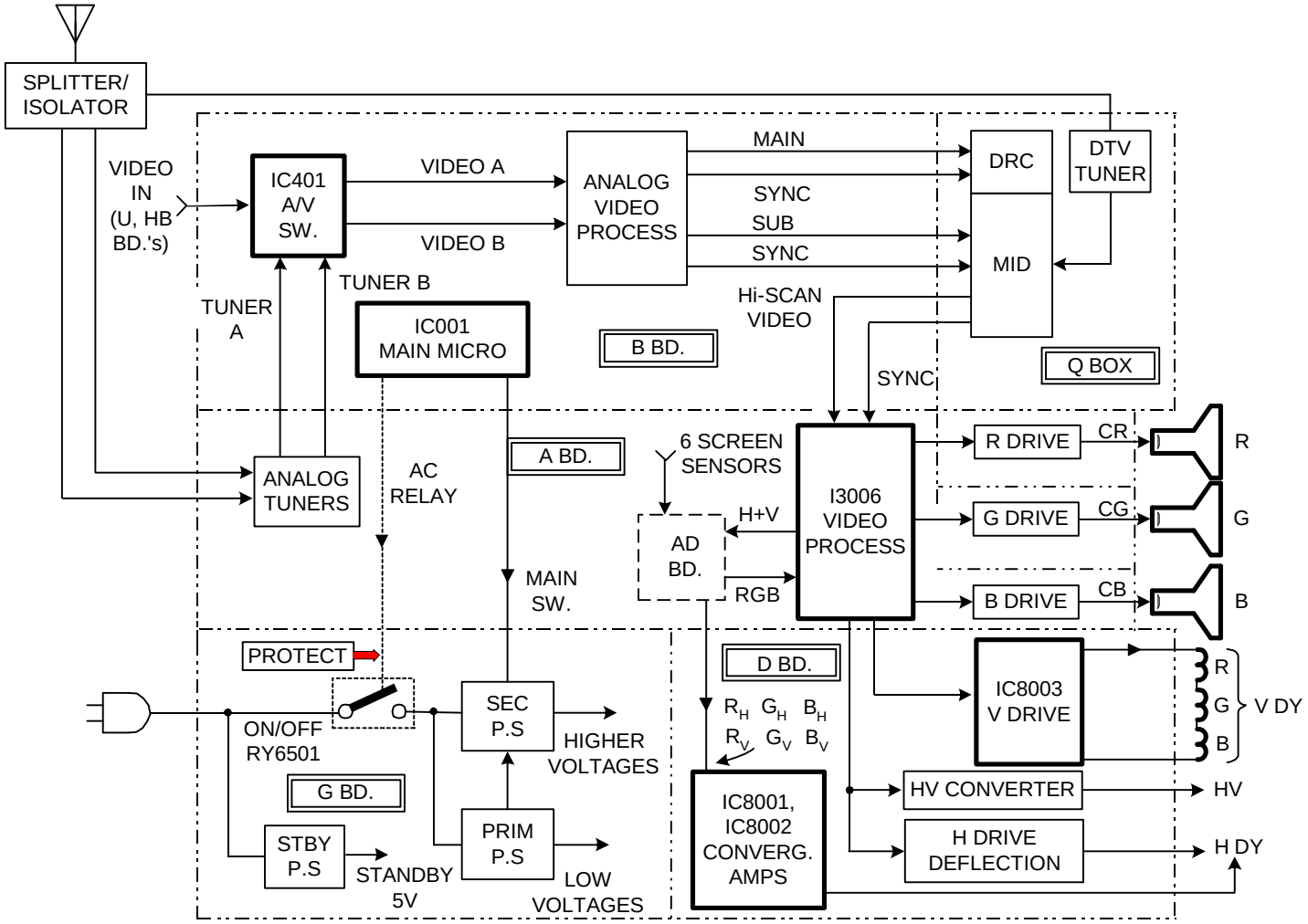


FIGURE 17-1- RA - 5A CHASSIS OVERALL BLOCK 49TVP12 1351 8/31/01

Power Supply

The entire low voltage power supply is located on the G board. The standby power supply delivers 5V to the Main Micro on the B board so it can respond to the power ON command form the remote or front panel. When the TV is turned ON, the Primary power supply delivers low voltages to the “Q” (DTV decoder) box, the A, AD and B boards.

Deflection and HV stage voltages (D board) are not present until the secondary power supply runs, so the TV is still dormant in its initial stage. The Main Micro and Primary power supply start the secondary power supply to complete the remainder of the voltages for set operation. The high voltage power supply starts after the horizontal deflection operates.

Deflection

When the Primary power supply runs, it develops voltage to start the horizontal and vertical oscillators in Video Processor IC3006 (A board). The horizontal oscillator from the A board is sent to the D board to produce the H Drive signal used by the horizontal deflection amplifiers and HV stage (D board).

The vertical stage also starts on the A board, but does not deliver its drive signal into the D board without communications from the Main Micro. The vertical oscillator IC3006 (A board) initially produces only vertical timing signals (VTIM is not shown) that are applied to Main Micro IC001 (B board). IC001 uses VTIM to output serial communications data and clock signal to ICs on the I^2C bus line during the vertical blanking time. This bus line includes IC3006, which originated the VTIM signal. When data and clock are received by IC3006, this IC can then output the vertical drive signal from the A board. The V drive feeds deflection IC8003 on the D board. This completes the vertical and horizontal deflection signal flow.

Video Process

The video processing encompasses the A, B, Q and the three C boards.

B board – Air or cable analog NTSC signal comes into the two tuners mounted on the A board before outputting composite video to the B board. The tuner video and video 1-6 is applied to A/V Sw IC401 for selection. Two selections are output. One will be used as the main picture and the other as the sub picture if the Twin View feature is called for. Both component video outputs are sent to the Q box.

Q Box - The main and sub component video and corresponding sync are sent to the DRC (main picture) and MID (sub picture) stages in the Q box. Here digital ATSC signals are received from the DTV tuner, processed and made available to the MID circuit for selection. The MID circuit chooses one (or two if in Twin View mode) and outputs a high-resolution video signal to IC3006 on the A board. The video signal was also changed so its frequency matches the 33.75kHz frequency of the horizontal oscillator in IC3006 (A board). Separate sync lines also go to IC3006 on the A board.

A board – Both sync and component video are sent to the A board. The V & H sync signals are applied to IC3006 for oscillator lock and to supply the convergence circuitry in the AD board. The component video is input IC3006 and converted to RGB. The RGB signal feeds the three CRT's cathodes.

Convergence

Convergence and Flash focus are independent operations sharing the same microprocessor and memory IC on the AD board. The AD board plugs into the A board.

Convergence – The purpose of this circuit is to modify the magnetic field in the main yoke of all three CRTs so their colored pictures become merged as one on the TV screen. There are two outputs from this board. One output is the main convergence signal consisting of RGB vertical and horizontal signals that feed the two convergence amplifiers on the D board. These convergence amplifiers output a final convergence signal that is applied to the convergence yoke within the main yoke. The second output is a pattern signal consisting of an RGB signal that is sent to Video Processor IC3006 for OSD. The pattern signal can be a crosshatch pattern for convergence or positioning boxes flash focus adjustment. Convergence settings are stored in a NVM IC within the AD board and shared with flash focus position information. This information should not be confused with Geometry settings for all three CRTs that are stored in a NVM (memory) on the A board.

Flash Focus – This user operation on the AD board automatically adjusts centering and now also adjusts size and linearity (new). The flash focus circuit produces a TV screen pattern using RGB output from the AD board into the A board's IC3006. The OSD positioning boxes are monitored by six sensors mounted at the screen edges to provide feedback to the AD board's flash focus circuitry for adjustment. The picture is converged and the centering, size and linearity data is modified in the memory on the AD board.

Power Supply Block (RA-5A Chassis)

The RA-5A projection TV chassis is similar in operation to the direct view HA-3 chassis, but the layout is confined to one board for simplicity. Refer to Figure 18-1 for a description of the power supplies and the power ON sequence.

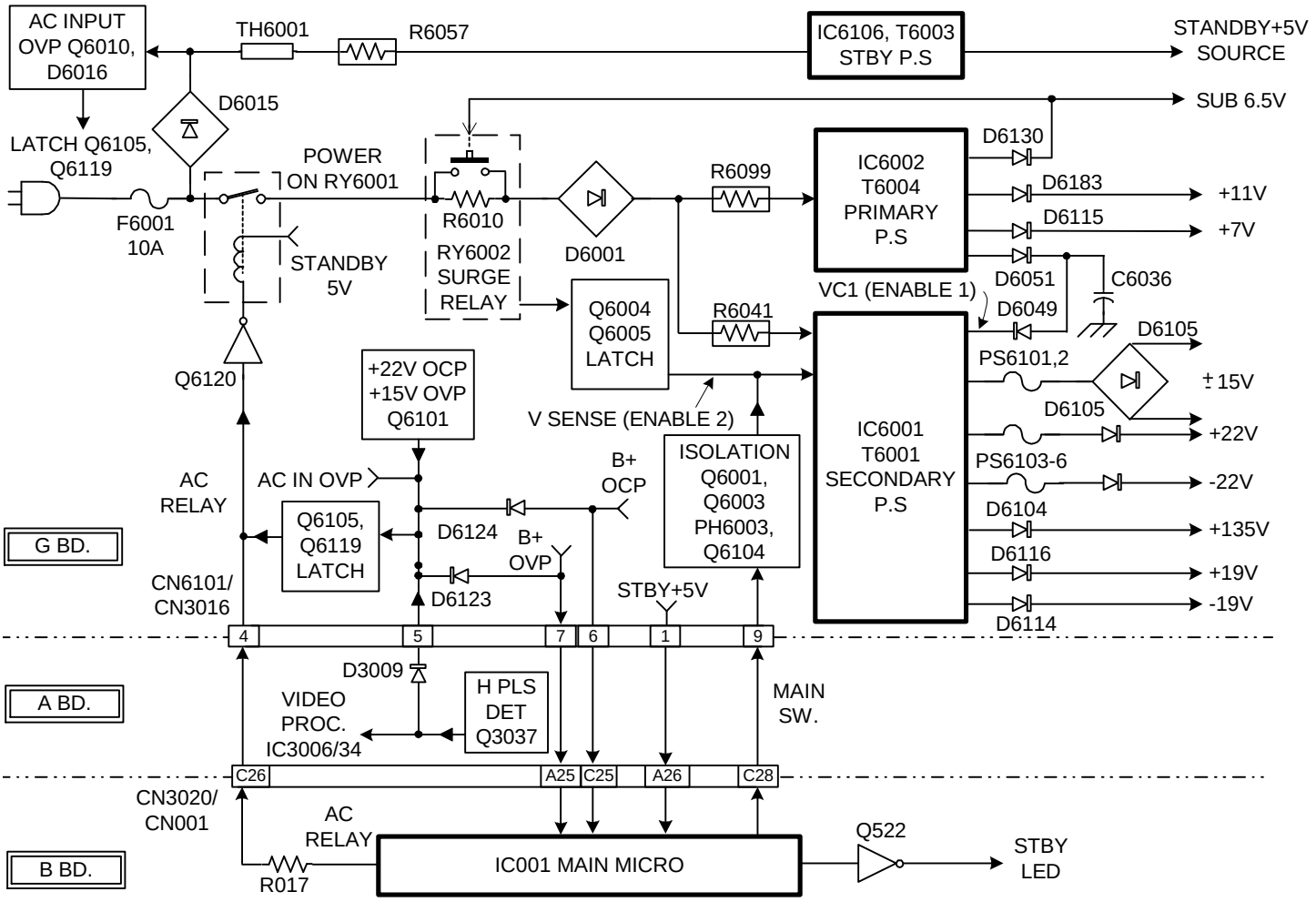


FIGURE 18-1 - POWER SUPPLY BLOCK - RA-5 A CHASSIS 21TVP12 1339 8/31/01

Power Supplies

Chart 18-1 shows that there are four power supplies found in the RA-5A projection TV chassis. Each power supply starts one at a time dependent upon prior stage operations for safety.

Chart 18-1 – RA-5A Power Supplies		
Name	Startup Requirements	Purpose
Standby	AC input	Standby +5Vdc for Micro IC001 on B board
Primary	AC relay (RY6001) & surge relay (RY6002) closes	?? Powers the Q Box and circuits on the A board. ?? VC1 Starts the Secondary PS.
Secondary	1) Primary PS outputs VC1 (HIGH at D6049) 2) Main Micro outputs Main Sw HIGH (CD6101/9) 3) Surge relay RY6002 must energize.	?? 135V for H Deflection, HV, Tuner (A & D Bd); ?? 22V for Convergence IC Amps (D bd ?? 15V for V Deflection and Op amps (D bd) ?? 19V for Audio Output (K Bd)
HV Converter (not shown)	1) 135Vdc (CN8013/9, D board) 2) 12Vdc (CN8016/1, D board) 3) H Drive (CN8006/10, D board).	Develops, regulates and checks the High Voltage to the three picture tubes.

Standby PS

This is a simple 60Hz step-down transformer power supply with a 5V regulator IC6106 at the secondary. The only unique part in this supply is the TH6001 thermistor in series with the primary winding. Since T6003 is working 24 hours a day, TH6003 prevents T6003 damage if the line voltage goes high for a prolonged time as commonly occurs during summer. If the abnormally high AC input voltage causes T6003 to draw more current, TH6001 will increase resistance to offset the current draw, preventing the transformer from over-dissipating. TH6001 measures 24 ohms cold and R6057 = 4.7 ohms.

The standby 5 volts can be easily checked at the G board's CN6101/pin 1. See Figure 18-2 for the G board connector locations. Pin 1 of each connector is at the right.

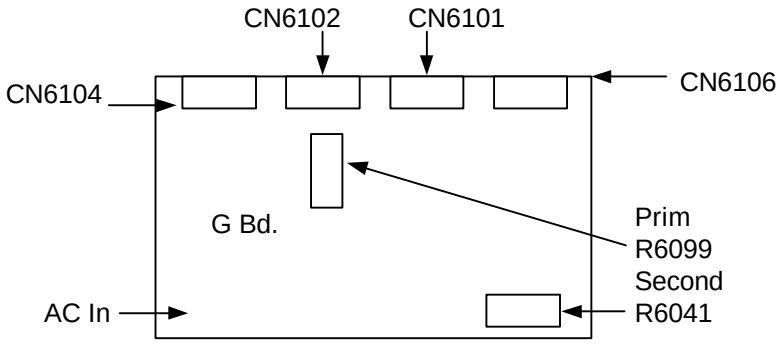


Figure 18-2 - G Board Connectors

Primary PS

The primary power supply starts as soon as the Main Micro IC001 B board turns on the AC relay RY6001. Only three voltages are output and are sent to the A board. From the A board, various voltages are sent to the QM, B and AD boards (final destinations). Chart 18-2 shows these destinations:

Chart 18-2 – Primary Power Supply Voltage Distribution G Bd to A Bd				
Primary PS Output	Location	A board Destination	Output	Final Destination
Sub 6.5V (digital)	CN6104/pin 8,9	CN3015/pin 1,2	6.5Vdc	QM board CN7001/pin 1,2.
11Vdc	CN6104/pin 1	IC3002 Regulator	9V	QM board CN7001/pin 9.
		IC3005 Sw Regulator	Sub 9V	B board CN3020//pin C4,5
			9V	A board IC3021 5V Regulator
7V or 6.5V (analog)	CN6104/pin 2,3	IC3003 Regulator	5V	QM board CN7001/pin 5.
		IC3007 Sw Regulator	5V	B board CN3020/pins C6,7
			5V	AD board CN3012/pin 17,

Secondary PS

The secondary power supply starts after being enabled by the primary power supply, the Main Micro and the surge relay. Figure 18-1 shows that the primary power supply makes VC1 to enable the secondary supply. The second enable line comes from the Main Micro IC001 as a "Main Sw" HIGH voltage (CN6101/pin 9 = 5V) about ½ second after power ON. The third enable comes from the surge relay RY6002. If the RY6002 contacts close before the capacitor in the Q6004/5 latch circuit charges, the latch does not activate and the V sense 2 line into the secondary power supply is enabled. The secondary power supply may now power up because its V Sense input is allowed to go HIGH.

All secondary PS outputs are fused, except the 19V and 135V lines. This power supply is connected to the D (deflection) and K (audio) boards. The D board supplies 15V and 135V to the A board. The destinations for the secondary power supply are listed in Chart 18-3.

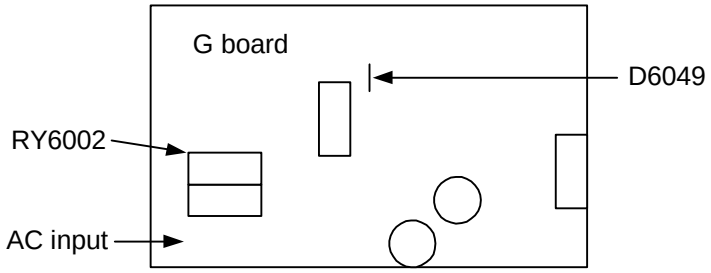
Chart 18-3 – Secondary Power Supply Voltage Distribution				
Primary PS Output	Location	D board Destination	Output	Final Destination
±15Vdc	CN6106/pin 1,3	IC8003 Vert Out		
		IC8004 Regulator	12Vdc	
		Through to A board	±15Vdc	A board CN8004/pin 8,10
19Vdc	CN610**2**/pin 7,8	Through to K board	19Vdc	K board CN2104/pin 7,8
±22Vdc	CN6106/pin 4,6	IC8001/2 Conv Amps		
135Vdc	CN6106/pin 9	H Drive, HV Conv		
		Through to A board	135Vdc	A board CN8006/pin 10

Power ON

The power ON sequence is similar to the HA-3 chassis (model KD34XBR2). Pressing the front panel or remote control ON button activates power ON. Main Micro IC001 responds by energizing the AC relay (RY6001), which powers the primary power supply. The primary power supply and Main Micro then turn ON the secondary power supply to supply the remaining power to the TV set for operation. The sequence is summarized in Chart 18-4.

Chart 18-4 - Power On Sequence		
Step	Action	Verification
1. Press Power On button	Main Micro receives the command	
2. AC Relay activates	Main Micro (B bd) activates AC relay RY6001 (G bd)	G board CN6101/pin 4 = 5Vdc
3. Primary PS powered	B+ applied to primary PS to start & run	G board CN6106/pin 8 or 9 = 6.5Vdc
4. Surge Relay activates	Primary PS output Sub 6.5 energizes surge relay RY6002	G board - Feel for click in rear relay RY6002. RY6001 is nearest the line cord.
5. Secondary PS is enabled 1.	VC1 voltage (15V) from Primary PS D6049/C enables the secondary PS.	G board - D6049/Cathode = 15.6V minimum
6. Secondary PS is enabled 2	Main Micro IC001 turns on Secondary PS.	G board CN6101/pin 9 = 5Vdc
7. Secondary PS powered	Secondary PS starts and runs powering TV	G board CN6106/pin 9 = 135Vdc
8. VTIM (vertical timing) pulses input Main Micro IC001	Video Processor (Jungle) IC3006 on A board gets 9Vdc operating voltage from Primary PS and outputs VTIM pulses to IC001 and IK test drive to CRT (in V blanking area of the CRT above the screen)	A board CN3014/pin 1 = 11V (regulated to 9Vdc on the A board)
9. Picture appears	Main Micro IC001 instructs Video Process IC3006 to output vertical drive and unblanks picture if IK signal is OK.	A board Serial data port CN3009/pins 10 (data), & pin 11 (clk).

FIGURE 18-3



G Board Tests (RA-5A Chassis)

Unlike other Sony projection TV chassis, the power supply in the RA-5A chassis will operate unloaded when turned ON. There are several ways you can power the G board, depending upon how much time you have: The first method is the fastest:

A. Power the G board and check output voltages (protection circuits operational).
B. Power Up the G board removed (protection circuits operational).
C. Powering up the G board power supplies after parts replacement.

A. Power the G board and check output voltages

Use this procedure to determine if the power supply G board is either being loaded down externally or is defective. The outputs from the G board can be unplugged and the TV powered ON to see if the G board is OK (can produce the normal output voltages).

Necessary Materials: 1k ohm resistor, DVM, remote.

Procedure:

1. Plug the TV set into AC and verify the Standby 5Vdc from the G board at CN6101/pin 1.
2. At the G board, unplug output voltage connectors CN6104 (to A board), CN6102 (to K board) and the CN6106 (to the D board). Leave control connector CN6101 plugged in.
3. Turn ON power from the remote or front panel. The power supply board will come ON and produce all voltages labeled at the connectors. The schematic and measured voltages are listed in Chart 19-1. Most voltages will remain at the terminals even when the TV is shut down because these lines are completely unloaded (unplugged). Cold ground is either at the connectors (labeled) or at the heat sink of D6105 near CN6106.

Chart 19-1 - Unloaded Output Voltages from the G board

Pin	CN6104 to A board		CN6102 to K board		CN6106 (to the D board	
#	Schematic	Measured	Schematic	Measured	Schematic	Measured
1	11V	11.3V *	11V	14.75V	-15V	-15V *
2	7V (A)	7.4V *	-15V	-14.2V	Gnd	
3	7V (A)	7.4V *	-15V	-14.2V	15V	14.75V
4	Gnd		Gnd		-22V	-22.5V
5	Gnd		Gnd		Gnd	
6	N/C		Gnd		22V	22.5V
7	Gnd		15V	14.15V	Gnd	
8	6.5V (D)	6.9V	15V	14.15V	N/c	
9	6.5V (D)	6.9V	* Unloaded. Needs to be manually discharged.		135V	135.3V
10		Gnd				

4. Sampling one voltage from each connector will only tell you if the primary and secondary power supplies are working. All voltages need to be measured because there are fuses on various lines. If the voltages are present, the G board is OK.
5. **Caution** - Before plugging the connectors back into the G board, you must discharge the unloaded voltages to avoid damaging parts. Touch a 1k-ohm resistor to the following * unloaded terminals and ground: CN6104/pin 1 (11V), CN6104/pin 2 (7V) and CN6106/pin 1 (-15V). Hold the resistor at each terminal for 10 seconds. The remaining voltages will dissipate within 10 seconds.

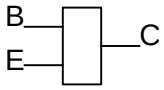
B. Powering Up the G board removed from the TV Chassis

When the board is removed from the chassis, the micro that turns ON the two power supplies must be simulated. Two jumper wires must be installed - the first to bypass the AC relay and the second to enable the secondary power supply. If good, the G board will then power up and produce all the voltages listed in Chart 19-1.

Required Materials: Soldering iron, short wires, AC cord, DVM, 1k ohm resistor.

Procedure:

1. Remove the G board. Be careful of the voltages across the larger capacitors (350Vdc max).
2. Plug AC into CN6001 (by the glass fuse).
3. Verify "Standby 5Vdc" from the G board at CN6101/pin 1.
4. Unplug the AC and place a jumper wire across CN6101/pins 1, 4 and 9.
5. Plug the board into AC. Both Primary and Secondary power supplies should work and you should be able to measure the voltages at connector CN6104 (chart 1). If the AC relay does not remain ON, the protection circuit has sensed a problem on the G board such as excessive output voltage or a defective latch.
6. To check the other voltages, the secondary power supply must be turned ON. Place a jumper wire across the B-E of surface package Q6003 (near heat sinked Q6007). See Figure 19-1 to locate Q6003.



7. Plug the board into AC. You should be able to measure the remaining output voltages (Chart 19-1).
8. **Caution** - Before plugging the connectors back into the G board, you must discharge the unloaded voltages to avoid damaging parts on the A and D boards. Hold a 1k ohm resistor to the following * unloaded terminals and ground. Connect the resistor at each terminal for 10 seconds. CN6104/pin 1 (11V), CN6104/pin 2 (7V), CN6106/pin 1 (-15V). The remaining voltages will dissipate within 10 seconds.

C. Powering up the G board power supplies after parts replacements

To avoid damaging the new parts installed to the primary or secondary power supplies, it is important to gradually apply power to the parts so you can detect a problem before the parts are damaged. In the following steps you will start the oscillator IC using an external power supply, then gradually bring up the input AC voltage with a variable AC transformer (Variac) while monitoring the AC input current and output voltage. The output voltage will be kept at a minimum by disabling the regulator circuit.

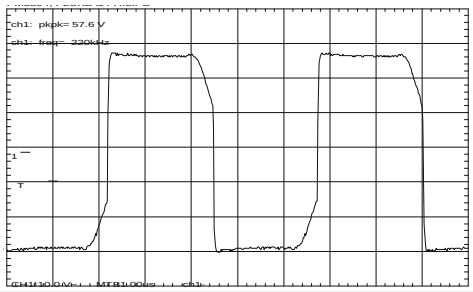
Needed Materials: Soldering iron, short wires, AC cord, DVM, 1k ohm resistor, 68k ohm resistor, diode, 16V DC power supply, AC Variac, scope.

Procedure:

Running just the Primary Power Supply

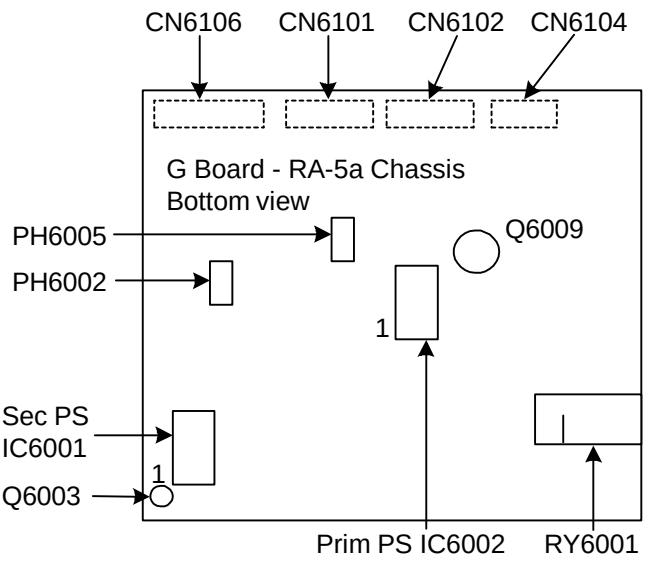
1. Place a jumper wire across the contacts of AC relay RY6001. See Figure 19-1 for the location of parts.
2. Short PH6005/pins 3-4 to disable the regulating circuit. This prevents the oscillator from pulsing on and off at low AC input voltages before regulation takes over.
3. Connect a 68k-ohm resistor between IC6002/pins 1 and 7.
4. Connect the band end of a rectifier/diode to IC6002/pin 7. The diode protects your power supply by preventing the TV's DC from entering your supply.
5. Connect the anode (unbanded) end of the diode to an external variable DC power supply.
6. The external power supply's negative lead goes to HOT ground at large cap C6010 neg. terminal or D6001's heat sink nearby.
7. Bring the external power supply to 12Vdc (23ma).
8. Connect one end of an AC line cord to CN6001 and the other to the AC Transformer (Variac) set to 0Vac.

9. Place your scope at Q6009/Drain of the primary power supply. Gradually increase the Variac voltage. The square Waveform 19-1 will start at 16Vac and gradually increase in amplitude. Make sure the waveform is flat on the top and bottom and its Vp-p is at the same level as the DC voltage from main rectifier D6001. For example at 20Vac, there is 60Vdc from D6001 and waveform should be 60Vp-p. Waveform 1 shows the square shape at 20Vac input to the TV.



Waveform 19-1 - Primary PS Output – 20Vac input			
	Name	Location	Voltage/div
Channel 1	IC6002 Output	Q6009/Drain	57Vp-p
Time base	1usec/div		
Waveform frequency = 220kHz			

Figure 19-1



10. Stop at each AC input level to recheck the output voltage and verify that almost no AC current is drawn. Only the primary PS voltages in Chart 19-2 will output. The frequency of the primary oscillator should remain at 220kHz as the input voltage increases because the regulator circuit has been disabled (step 2).
11. Finally, test the regulating circuit by measuring the voltage across PH6005/pins 1-2 with the board powered up. 0V = normal. 1.2V or higher means the regulating IC6107 is defective.

Chart 19-2 – Primary and Secondary Output Voltages at various input voltages					
AC Input Voltage	20Vac	30Vac	50Vac	90Vac	120Vac
D6001 Output	60Vdc	87Vdc	146Vdc	254Vdc	336Vdc
Primary PS					
CN6104/pin 1 (11V)	1.86Vdc	2.38Vdc	4.1Vdc	6.24Vdc	7.8Vdc
CN6104/pin 2 (7V)	1.1Vdc	1.55Vdc	2.7Vdc	4.6Vdc	5.8Vdc
CN6104/pin 8 (6.5V)	0.72Vdc	1.1Vdc	1.96Vdc	3.5Vdc	4.6Vdc
Secondary PS					
CN6106/pin 9 (135V)	18.55Vdc	25.3Vdc	44.4Vdc	79Vdc	108Vdc
CN6106/pin 6 & 4 (±22V)	±3Vdc	±4.16Vdc	±7.6Vdc	±13.46Vdc	±18.3Vdc
CN6106/pin 3 & 1 (±15V)	±2Vdc	±2.8Vdc	±5Vdc	±8.8Vdc	±12Vdc

Running both the Primary and Secondary Power Supply

12. Unplug the AC and disconnect the DC voltage to the blocking diode.
13. Move the resistor and diode from IC6002/pins 1 and 7 to IC6001/pins 1 and 7.
14. Short Q6003/ base to emitter. This enables IC6001.
15. Move the short from across PH6005/pins 3-4 to PH6002/pins 3-4.
16. Place the scope probe at Q6007/Source to monitor the oscillator output.
17. Connect the DC power supply to the blocking diode that is soldered to IC6001/pin 7.

18. Set the DC power supply to 16Vdc. More voltage (15.6Vdc) is required to start this IC because pin 18 is not connected to a Vcc source.
19. Plug the AC cord to the Variac and bring up the voltage slowly as with the primary power supply. The secondary voltages in chart 2 will appear as you increase the AC input voltage. The secondary PS oscillator frequency should remain stable at approx. 183kHz.
    Note that at about 87Vac, the Primary power supply will suddenly turn ON full and its 11V line will energize the Surge relay (click sound). This is normal, so do not be startled. The primary power supply will deliver these voltages from CN6104 unloaded:

- CN6104/pin 1 (11V output) = 11.3Vdc;
- CN6104/pin 2 (7V output) = 7.4Vdc;
- CN6104/pin 8 (6.5V output) = 6.9Vdc

Protection Block (RA-5A Chassis)

Refer to Figure 20-1 for an overview of the protection circuits.

When a serious problem occurs, this TV will protect the remainder of its circuitry and the picture tubes in one of the following ways:

- TV shutdown (AC relay is turned off);
- TV Latched OFF (AC relay is held off); or
- Picture is blanked to produce a dark screen (no RGB signal to the CRT cathodes).

When the TV is placed in one of these protective states, IC001 also indicates the cause by blinking the Standby LED a number of times, pauses, and then repeats the same count.

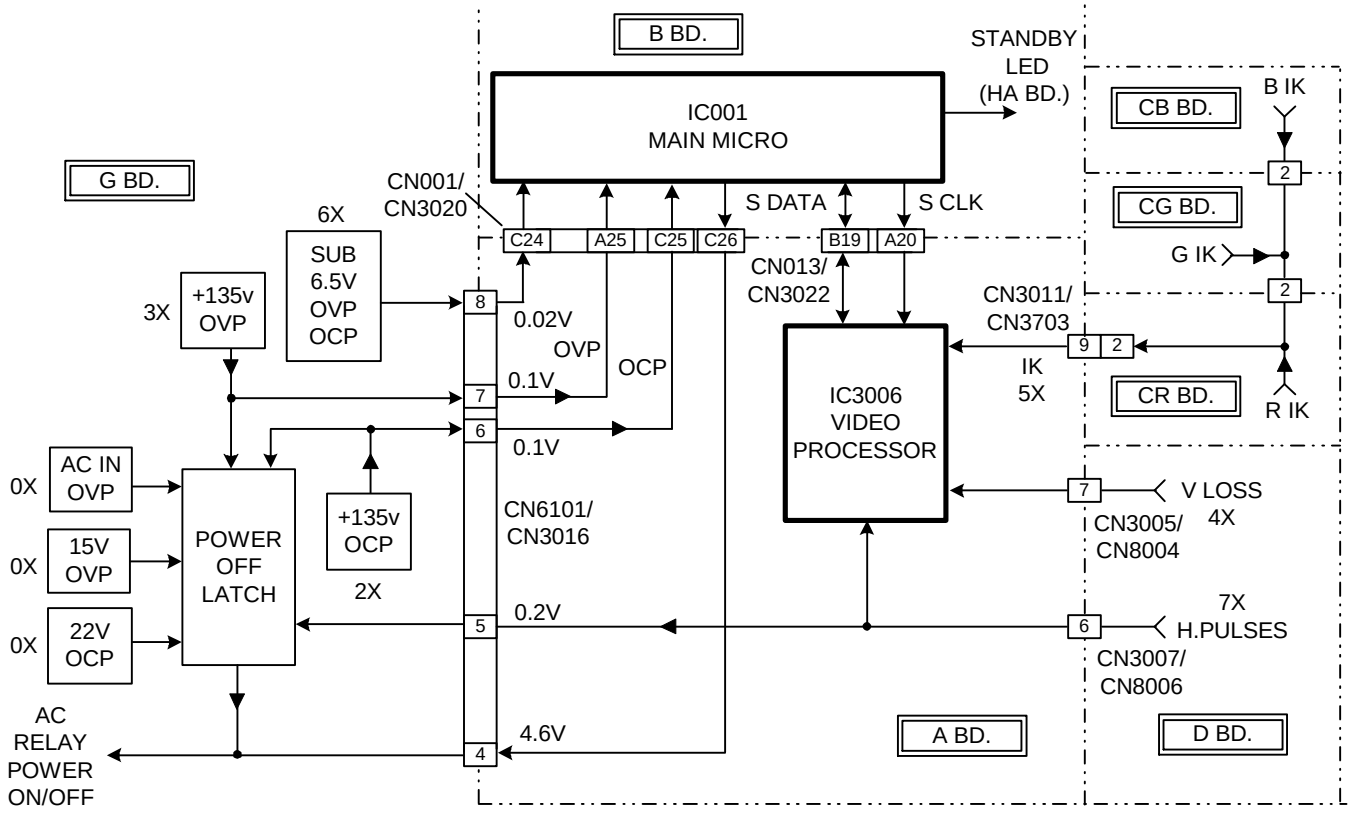


FIGURE 20-1 - PROTECTION BLOCK - RA-5A CHASSIS 33TVP 1351 9/4/01

Chart 20-1 summarizes the TV's seven protected areas. Use Chart 20-1 and Figures 20-2 and 20-3 to verify the signal that triggered the protection (shutdown). If no signal triggered the protection, suspect Micro IC001 on the B board and the latch transistors (Q6105/Q6119) on the G board of causing the TV shutdown.

Chart 20-1 - Shutdown Causes				
Stby LED Blinks	Protected Area		Shutdown Verification	
	Circuit	Bd	Location	Normal Voltage
0 X	+AC line OVP, 15V OVP, 22V OCP	G, D	G Bd - PH6004/ pin 3	0.1Vdc
2 X	+135V OCP	D	CN6101/ pin 6	0.1V
3 X	+135V OVP	D	CN6101/ pin 7	0.1V
4 X	V Out Loss	D, A	D Bd - CN8004/ pin 7	5Vp-p Pulses at V rate
5 X (pix blanked -TV remains ON)	IK balance	C/A /G2 adj	A Bd – CN3011/ pin 9 or CR Bd CN3703/2	3 pulses in vertical interval.
6X	Q6.5V OVP & OCP	Q box , G	G Bd - CN6101/ pin 8	0.1Vdc
7X	H Out Drive	D, A	D Bd - CN8006/ pin 6	H pulses 5Vp-p

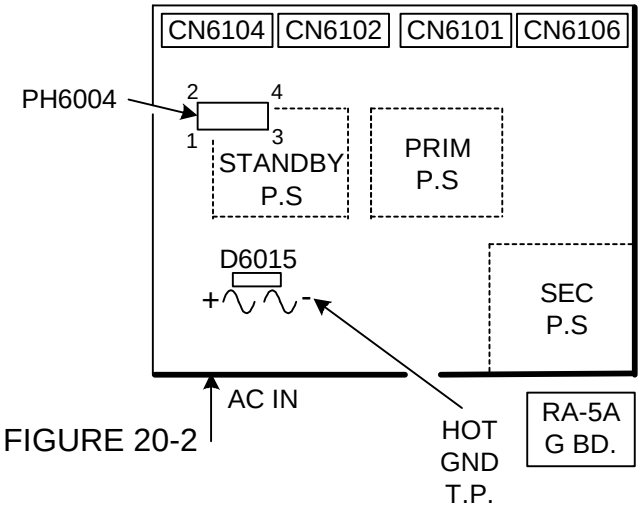


FIGURE 20-2

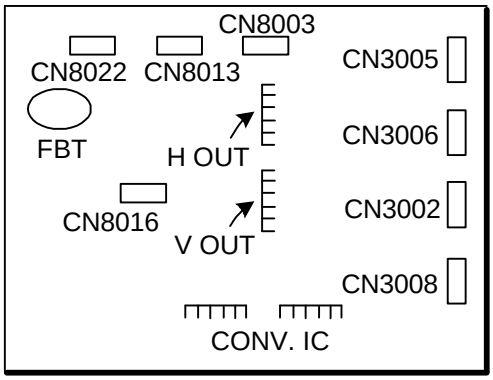


FIGURE 20-3

Protection Circuits

After the TV enters a protective state, the standby light blinks to identify one of seven problem sections. The problem section not only consists of the protected circuit (load), but also the sensing circuit that monitors the fault. In the following seven sections, there is a description of the sensing circuit itself so you know how the load is being protected and a test procedure to determine if the board that contains the load or circuit is at fault.

Standby light blinks 0 times – TV Shutdown

Refer to Figure 20-4 for the Circuit description and the Testing procedure that follows.

Circuit – When the TV shuts down (no line current) and the Standby light does not blink (indicates the trouble area), three protection circuits are suspect:

- AC Input OVP
- +15Vdc OVP
- +19Vdc OCP
- +22Vdc OCP

The first two areas are most likely confined to the G board. The 19Vdc and 22Vdc OCP is likely to be a D board problem.

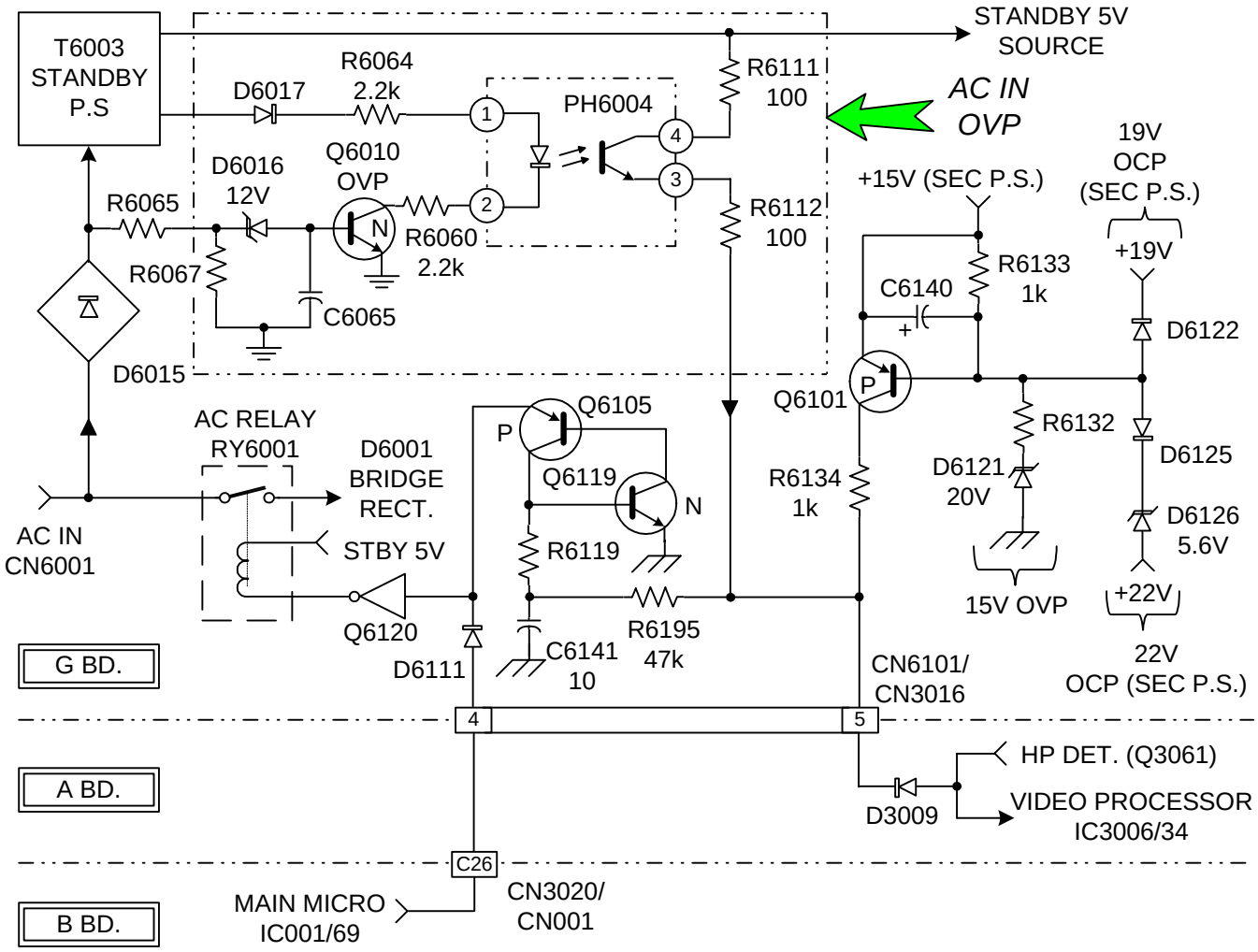
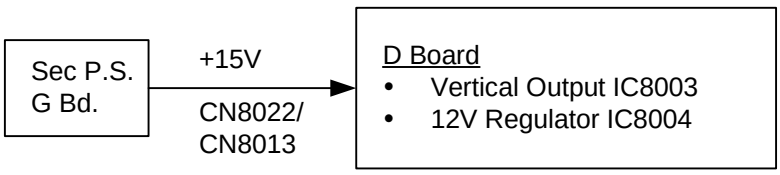


FIGURE 20-4 - SHUTDOWN - NO INDICATION - RA-5 CHASSIS 27TVP12 1344

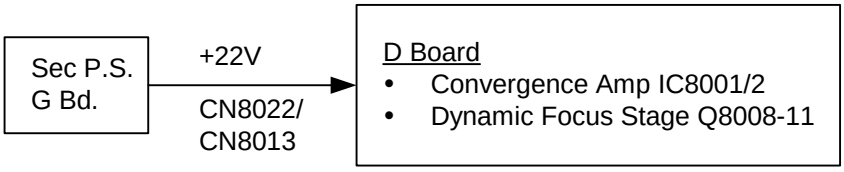
1. AC Input OVP – D6016 and Q6010 monitor the DC voltage from bridge rectifier D6015 that corresponds to the AC input voltage. If the AC input reaches a trip voltage of 165Vac, Q6010 turns on opto isolator PH6004. PH6004/ pin 3 outputs a HIGH that turns on latch Q6105/Q6119. This two-transistor latch grounds out the AC relay drive voltage at CN6101/pin 4 to prevent the AC relay from turning ON so the TV shuts down.

2. +15Vdc OVP - The 15Vdc line from the secondary power supply (IC6001) on the G board is monitored by Q6101 and zener D6121. If the 15V line rises to 20.6Vdc, Q6101 turns on latch Q6105/Q6119. This latch removes the AC relay voltage and the TV shuts down from the excessive voltage. The cause for excessive +15V is poor or no regulation in the secondary power supply, or a loss of load. The major load for the 15 line is the circuitry on the D board.



3. +19Vdc OCP – The 19Vdc line is from the secondary power supply. The load is the audio output stage. If the 19-volt line were loaded down, its voltage would drop. If it drops below 15Vdc, D6122 and Q6101 turn ON to trip the latch formed by Q6105 and Q6119. This latch shuts down the TV.

4. +22Vdc OCP – The +22Vdc line from the secondary power supply (IC6001 – G board) supplies the convergence amplifiers and the Dynamic Focus circuitry on the D board (not shown). D6126 and Q6101 monitor the +22V on the G board for low voltage. This circuit would shut off the TV if the 22-volt line dropped to 8.2Vdc.



Testing – If the TV Power ON and Surge (not shown) relays turn ON but quickly turn back off with NO standby light indication, use figure 20-5 to determine which one of the four circuits is causing the shutdown:

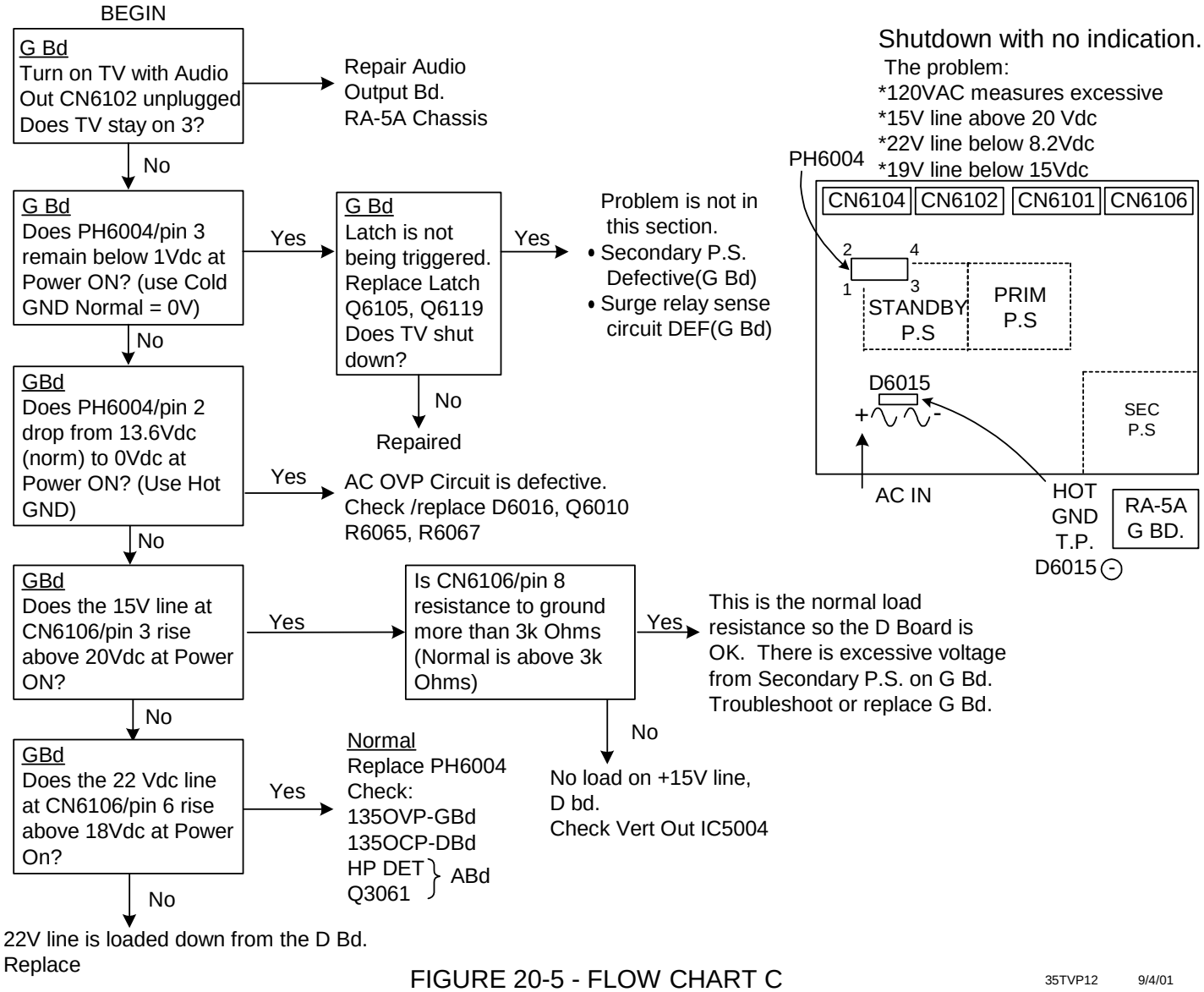


FIGURE 20-5 - FLOW CHART C

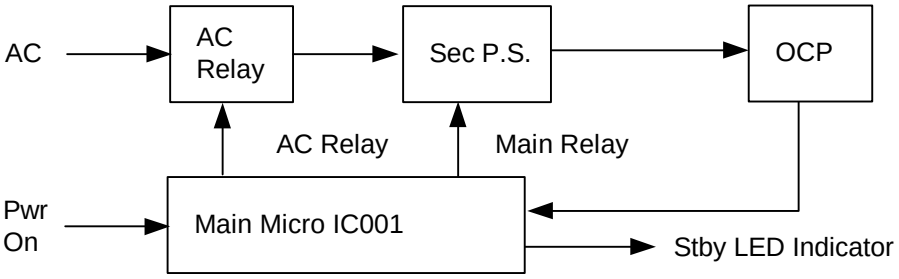
35TVP12 9/4/01

There is also a possibility that a simultaneous loss of communications from the B (IC001) to the A board (IC3006) and loss of horizontal drive will result in shutdown without a blinking LED, possibly from a broken or contaminated A board. See Standby light blinks 7X or the overall protection block diagram 33.

Standby light blinks two times – TV Shutdown

The +135V OCP monitoring circuits are located on the G board, but the indicating circuit is on the B board. This circuit monitors current drawn by the horizontal regulator that provides power for the horizontal output stage. See Figure 20-6 below:

Figure 20-6



Circuit - Refer to Figure 20-7 for the following circuit description of the 135V load and current sensing circuit.

135V Loads (D, C, A and V boards)

The 135V OCP circuit monitors the current on the +135V line from the Secondary Power Supply to the D, C, A and V boards. Of all the +135 volt line loads listed, the D board is the most demanding:

- Horiz Output (Q5030) and PWM (Q5003) stage (D board).
- The HOT on the D board in turn supplies +200V to the RGB Video Output ICs (C board).
- 33V tuning voltage to analog tuners (A board).
- Velocity modulation coils (V board).

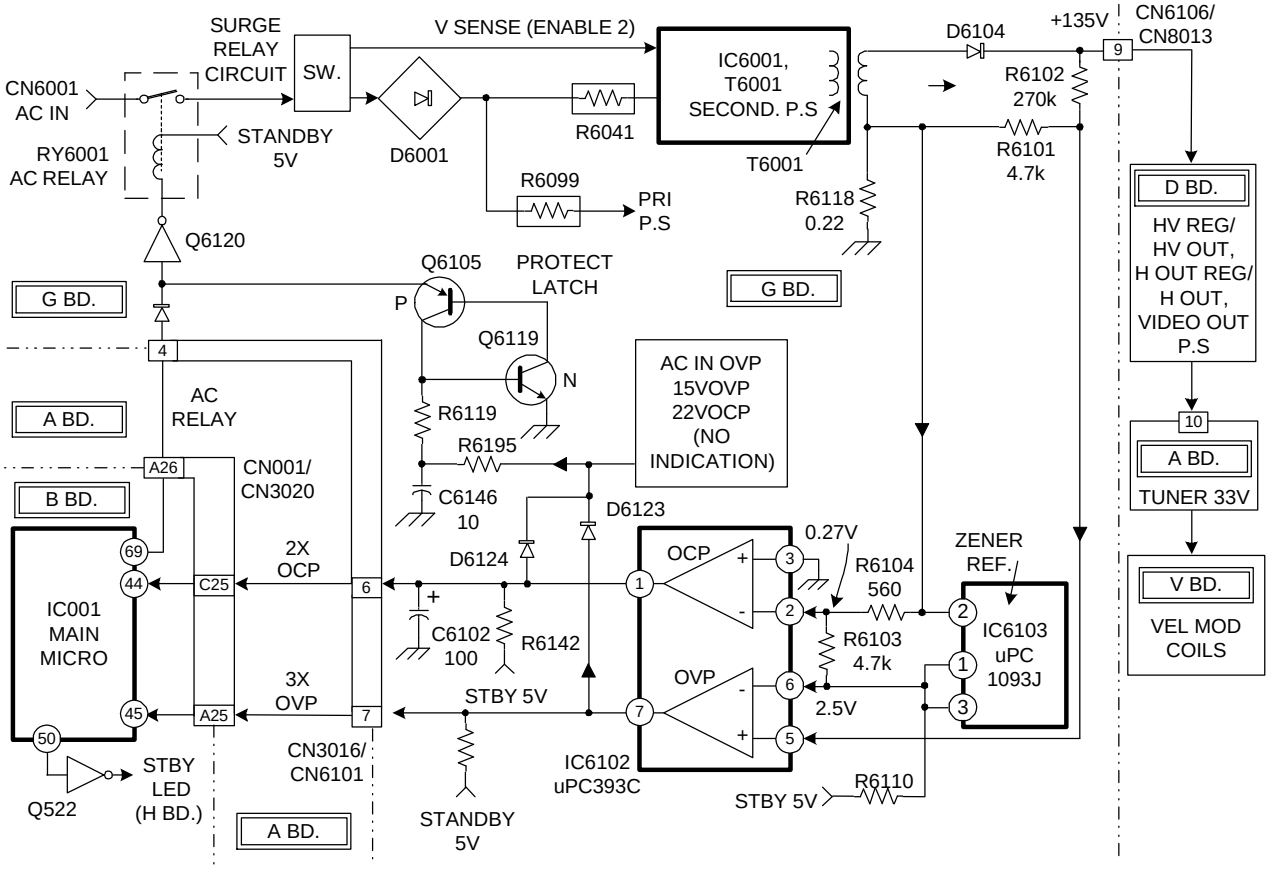


FIGURE 20-7 - PROTECTION - 2X, 3X INDICATION - RA-5 CHASSIS 28TVP12 1345 9/4/01

135V Current Sensing Circuit (G board)

The 135V sensing circuit consists of R6118 and IC6102. R6118 is connected to the 135V line at the ground end. As the current along the 135V line increases, the voltage across R6118 becomes negative (similar to ABL voltage). This negative voltage that represents the 135V-line current offsets the 0.27V at comparator IC6102/pin 2. When the voltage at IC6102/pin 2 drops to the same voltage as pin 3 (0V), the output pin 1 goes HIGH to shut down the TV and light the standby light.

The HIGH from comparator IC6102/pin 1 is split into two paths. One path is through D6124 to trip the Q6105/Q6119 latch that shuts off the TV. The other path is through CN6101/pin 6 to inform the Main Micro IC001 that the 135V line current has exceeded 0.7A. IC001 will indicate the 2X-blink failure code as long as the TV is plugged in.

Testing – You can determine if the sensing circuit or the load is defective by removing the load, but you must keep the error regulating circuit on the G board operational. L6106 is in series with the 135V output connector CN6106/pin 9. Removing L6106 removes all the loads. You should then power up the TV to see if the standby LED still blinks two times. It will usually stop blinking two times, meaning you disconnected the problem but the TV will still shut down and blink seven times because there are no H pulses.

The problem has been isolated to load on either the D, C, A or V boards. See Figure 20-7. The +135Vdc leaves the G board and goes to the H. Regulator and Output stage load on the D board and the velocity modulation coils on the V board. Attack the D board first by testing the H Out transistor (Q8024), and the H Regulator output transistor (Q8027). A similar circuit description and simplified schematic of an H. Regulator and Output stage is in the DTV-02 training manual on page 37. The V board can be unplugged and the zener on the A board could not cause the TV to enter shutdown. Reinstall L6106 onto the G board.

If the LED still blinks 2X with the load disconnected (L6106 removed), the problem is on the G board sensing circuits. Suspect IC6102, IC6103 and R6118.

Standby light blinks three times – TV Shutdown

Refer to Figure 20-7, for the following 135V OVP circuit explanation and testing.

Circuit –The +135 voltage limit is 150Vdc. This limit is checked by R6101, R6102 and IC6102. Normally with an output of 135V, the junction of the R6101/R6102 voltage divider produces 2.3Vdc into IC6102/pin 5. This 2.3V is compared to the 2.5Vdc reference voltage placed at pin 6 by IC6103. Because the 2.3Vdc applied to the + input of Op Amp IC6102/pin 5 is lower than its input at pin 6, the output at IC6102/pin 7 will be 0Vdc. However, if the 135V line rises to 150Vdc, its corresponding voltage at IC6102/pin 5 will increase from 2.3V to meet the reference voltage of 2.5V. IC6102's output at pin 7 will go HIGH. The HIGH that outputs IC6102/pin 7 is applied to the Q6105/Q6119 latch that shuts off the TV set. The HIGH also goes to IC001 via CN6101/pin 7 causing the standby LED to blink three times repeatedly.

Testing - To verify the defective condition on the G board, monitor the 135V line at CN6106/pin 9. If this line rises above 135V at turn ON, the secondary power supply or its regulator (G board) is at fault.

If the 135V line did not rise above the limit, this 135V OVP sensing circuit is defective. Measure the shutdown latch trip voltage at CN6101/pin 7. At power ON this voltage normally remains at 0Vdc. If this line rises above 0.7Vdc, then suspect IC6102 and IC6103. All these circuits are on the G board.

Standby light blinks four times – TV Shutdown

Refer to **Figure 20-8** for this circuit description and testing.

Circuit - A Vertical Output IC failure or secondary power supply failure (both on the D board) will stop vertical pulses from being detected at IC3006/pin 35. This loss will cause IC3006 to blank the screen (no RGB output) and emergency serial data will be sent to Main Micro IC001 (B board). IC001 turns the TV OFF by dropping the AC relay drive voltage (IC001/pin 69 goes LOW) and blinks the LED four times.

Testing - At power ON, verify +15v and -15V to the vertical output IC5004/pins 2 and 4. This voltage comes from the secondary power supply on the G board. Then look for vertical drive signal at CN8006/pin 3 and 5. It is possible to have reduced vertical deflection if one drive input is missing.

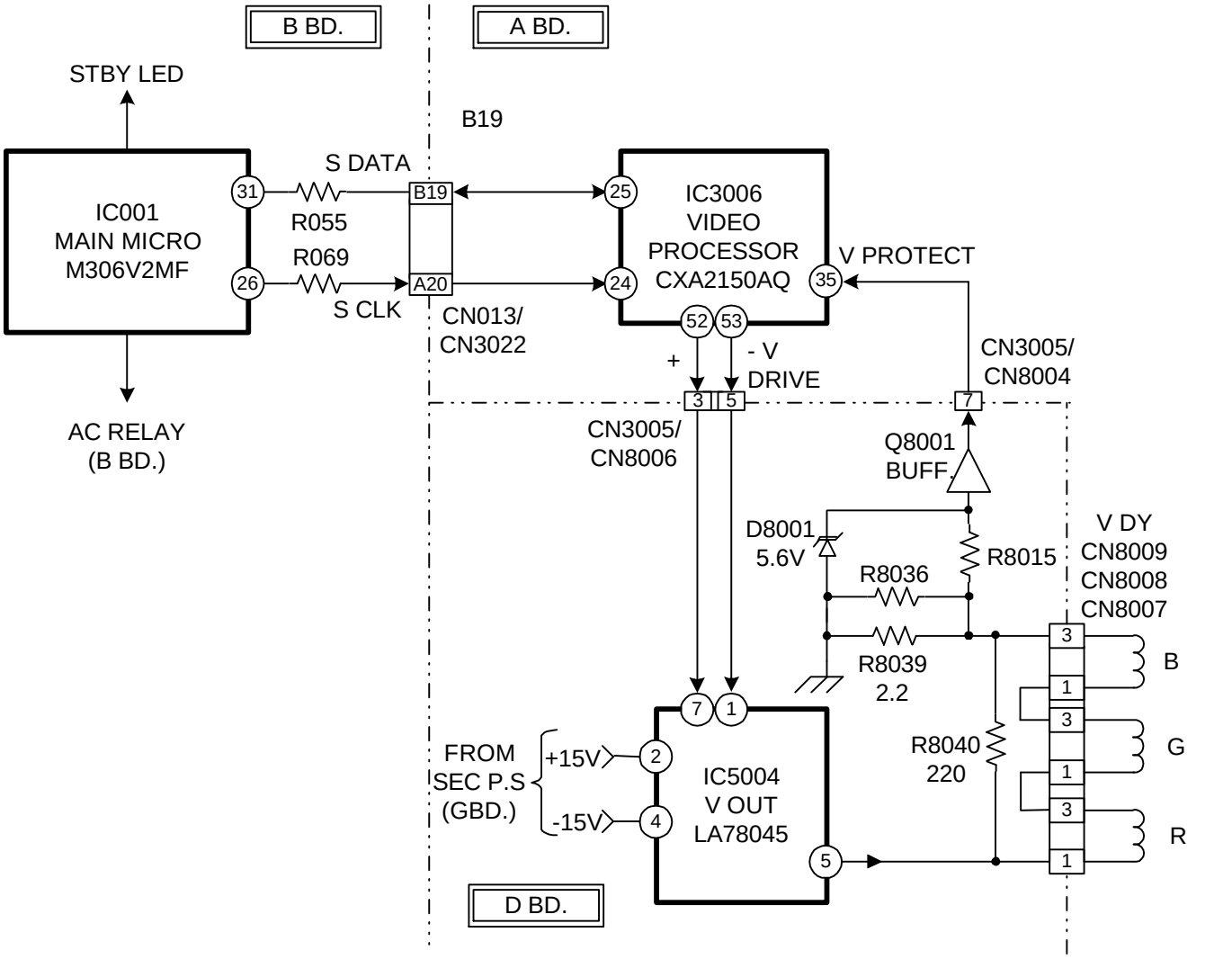


FIGURE 20-8 - PROTECTION - 4X INDICATION - RA-5 CHASSIS 30TVP12 1346 8/31/01

Standby light blinks five times - Blanking

Refer to Figure 20-9 for this circuit description and testing.

Circuit - Three IK pluses are measured by Video Processor IC3006 as they return into pin 58. Each pulse corresponds to the efficiency of each CRT cathode and therefore is used to adjust the RGB gain within IC3006 to maintain color balance while the TV is operating (dynamic adjustment). The IK signals originate from IC3006 as three bright lines in the vertical-blanking interval at lines 19-21. As the picture tube ages, the Ik signals may fall below the threshold for automatic balance adjustment, causing IC3006 to mute/blank the substandard picture. Although the picture is blanked, the IK pulses still output IC3006 and the three return IK pulses to IC3006/pin 58 are still operational as long as the TV is ON.

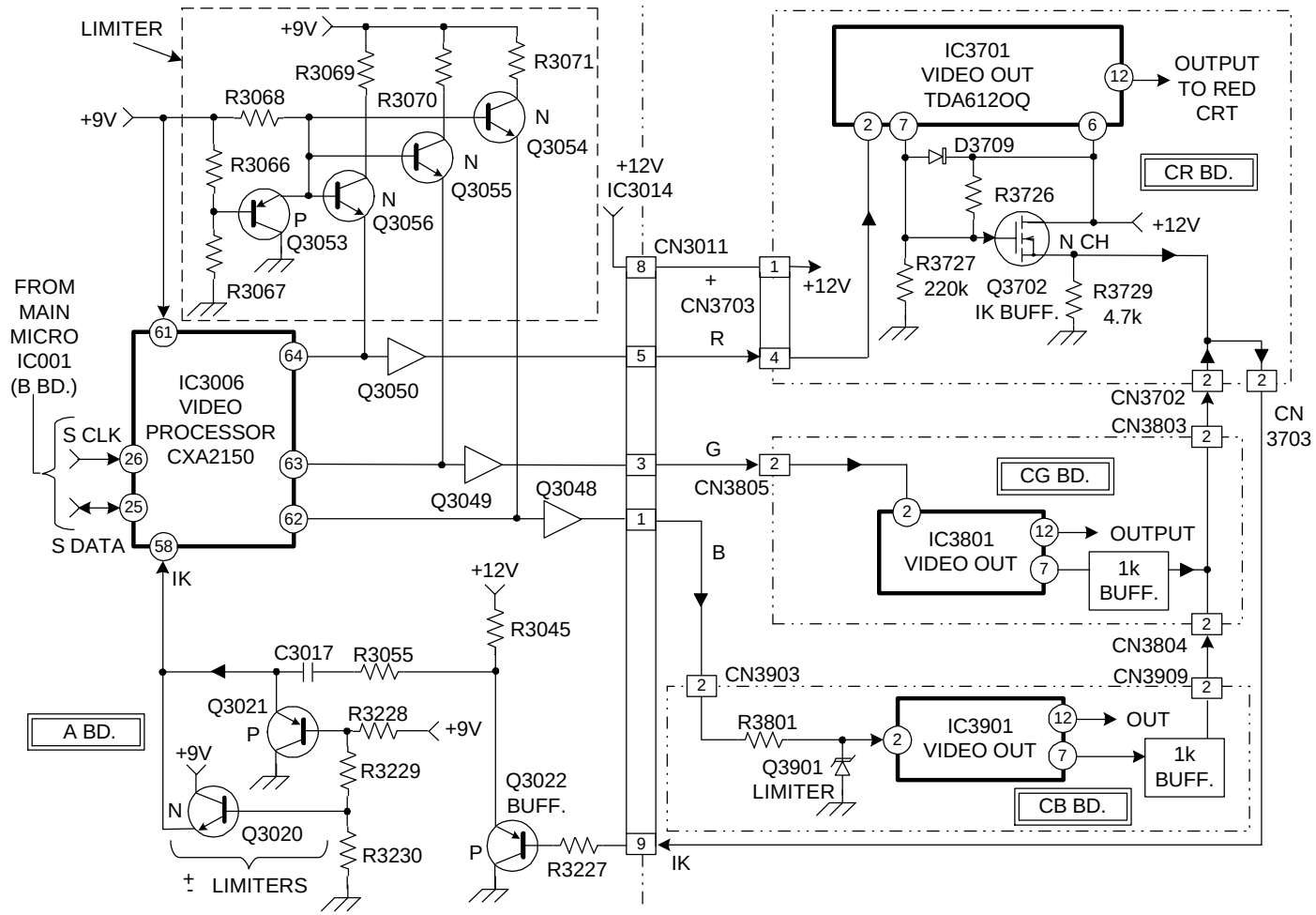


FIGURE 20-9 - PROTECTION-5X INDICATION - RA-5A CHASSIS 31TVP12 1348 9/4/01

Testing - Increase the G2 control on the CRT's C board. If that does not return cathode current to within operating range so the picture appears, examine each filament to see if it is lit.

Then use your scope to examine the signal at the cathode. Go to CN3011/pins 1, 3 and 5 to see if there is a drive signal going to the C boards. Next, check for these signals at each CRT cathode. If they are present, examine the IK signal into the A board at CN3011/pin 9. You should see three pulses that change in level as the G2 control is adjusted. One pulse corresponds to one color and should be within 15% of each other. The normal IK output from the CRT/C board is about 1Vp-p pulses at pin 9. If these three pulses are present at pin 9, the problem is on the A board about IC3006.

Standby light blinks six times – TV Shutdown

Refer to Figure 20-10 for this circuit description and testing.

Circuit – IC001/pin 43 monitors the Sub 6.5Vdc from the Primary power supply (G Bd) to the Q box (QM and QI boards). A short or excessive voltage on the Q6.5Vdc line will cause IC001 to shut off the AC relay (IC001/pin 69 goes LOW), shutting down the TV and blinking the LED six times.

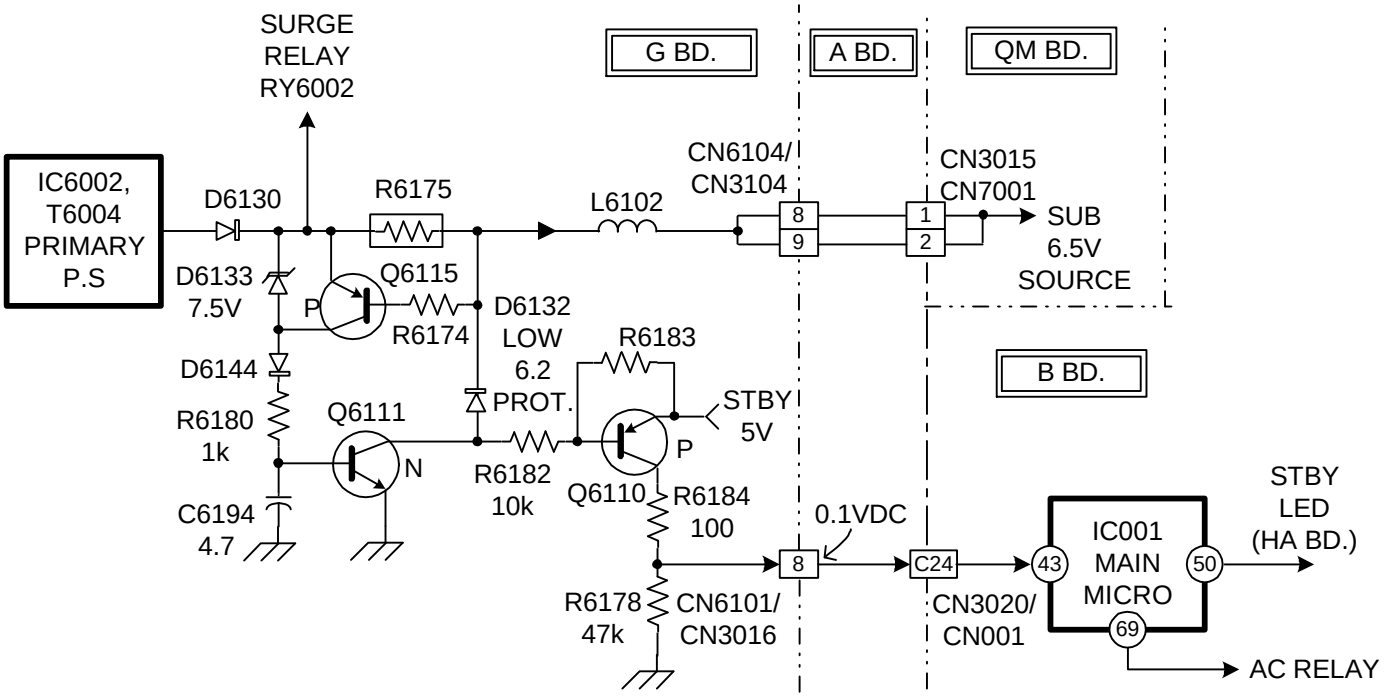


FIGURE 20-10 - PROTECTION - 6X INDICATION - RA-5A CHASSIS 32TVP12 1349

Testing – Unplug CN7001 to the Q box (consists of QI and QM boards) and power On the TV. Normally the TV will power ON with HV, a dark screen and no sound because there is no microprocessor-to-microprocessor communications. If the TV does not shut down, the problem is in the Q box because you unplugged the short. If the TV still shuts down, the problem is in the primary power supply (G board). Measure "Sub 6.5Vdc" at D6130 cathode on the G board at power ON. A high of 8Vdc will trip the protection latch and shut down the TV. The TV will not display A/V without the Q boards active, but will remain ON.

Standby light blinks seven times – TV Shutdown

Refer to Figure 20-11 for the circuit and testing of the Horizontal sweep detection circuit.

Circuit – If the horizontal sweep is lost for a moment, three vertical lines would instantly appear on the three CRTs and burn a line into the tubes. To prevent this, a horizontal activity circuit consisting of D3011, C3090, R3140 and Q3037 keep IC3006/pin 34 LOW as long as horizontal pulses are fed into the circuit.

Horizontal pulses into the activity circuit come from the horizontal Output transistor Q8024/Collector. A capacitor voltage divider (C8096-8) reduces the 1KV, 31.5kHz spikes. The horizontal spikes are clamped (limited) and shaped into rectangular pulses by zener D8026. Buffers Q8031/Q8101 apply the reshaped pulse to the horizontal activity circuit. D3011 is the first part of this circuit outputting a DC voltage to LPF C3090/R3140. The DC voltage keeps Q3037 turned ON. When Q3037 is ON, IC3006/pin 34 remains LOW for normal operation.

During a defect when horizontal pulses are NOT detected, IC3006/pin 34 goes HIGH. This HIGH is used to blank the screen, trigger the Standby LED indicator and shut down the TV. IC3006 blanks the RGB output in its own IC and sends data to instruct Main Micro IC001 to blink the standby LED seven times. The HIGH is also applied through D3009 to the latch circuit on the G board to shut down the TV for safety.

The protect Mute line from IC001/pin 67 places a HIGH at Q3037/base for five seconds at power ON to prevent this circuit from shutting the TV back off after turn ON.

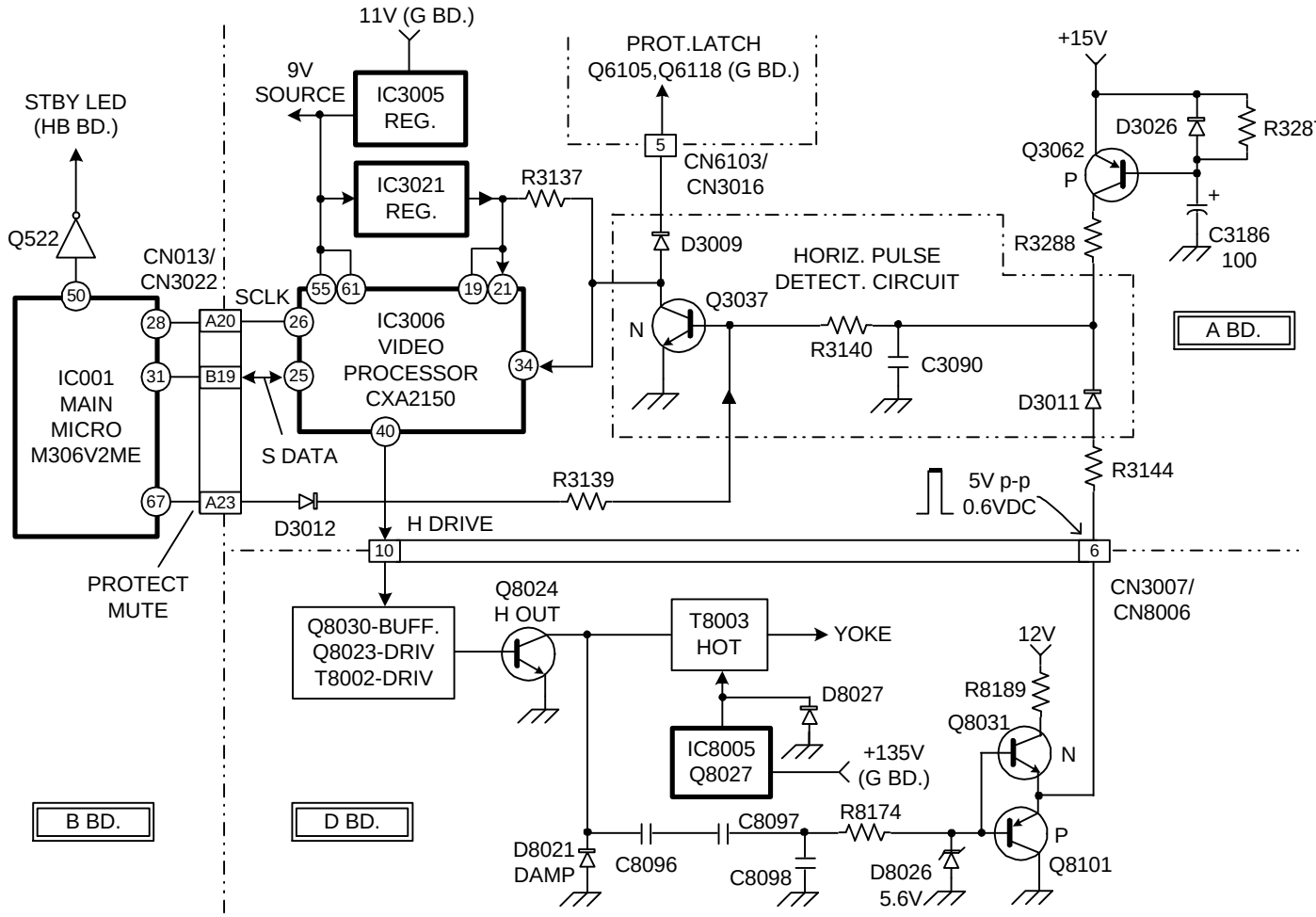


FIGURE 20-11 - PROTECTION 7X INDICATION - RA-5 CHASSIS 29TVP12 1347 9/4/01

Testing - If the Standby light blinks seven times, the problem is most likely on the D board where the Horizontal Regulator and Horizontal Output stages are. Use this three-step method to determine if the problem is on the G, D or A board:

1. On the D board CN8013/pin 9, verify there is 135V coming into the D board from the G board.
2. On the D board, look for 5Vp-p H drive pulses into the D board at CN8006/pin 10 from the A board.
3. On the D board, look for 5Vp-p H pulses output from the D board at CN8006/pin 6 into the A board.
   Not Present - The problem is on the D board, suspect the Horizontal Output (Q5030), PWM (Q5003/Q5011) transistors on the D board and video output ICs (C board).

   Present - The D board is OK and the problem is in the sensing circuit on the A board. Suspect components D3011, C3090, R3140 and Q3037.

High Voltage Stage (RA-5A Chassis)

HV Power Supply Start Up (Board level repairs)

As shown in Chart 21-1, the HV stage starts when enabled by three inputs.

Chart 21-1- HV Stage Inputs (for Starting)		
Name	From	Checkpoint
1. +135Vdc	D6104 / cathode (G Bd – Sec PS)	Q8035/ S (D Bd)
2. +12Vdc	12V Reg IC8004 / output (D Bd)	IC8008/1 (bottom) or (CN8016/pin 1, 2)
3. H Drive	Video Process IC3006/pin 40	CN8006/pin 10

Once these three voltages are present, there is no reason the HV should not start unless the D board HV circuitry is defective. See Testing for the procedure and location of the checkpoint connectors.

The HV stage can be tested for operation and level by measuring the sample of the HV at:

CN8016/pin 3 = 7.46Vdc. See Figure 21-2 for the schematic and “Testing” for connector locations.

HV Block Description (Component level repairs)

The HV Stage only has a few major blocks as shown in Figure 21-1.

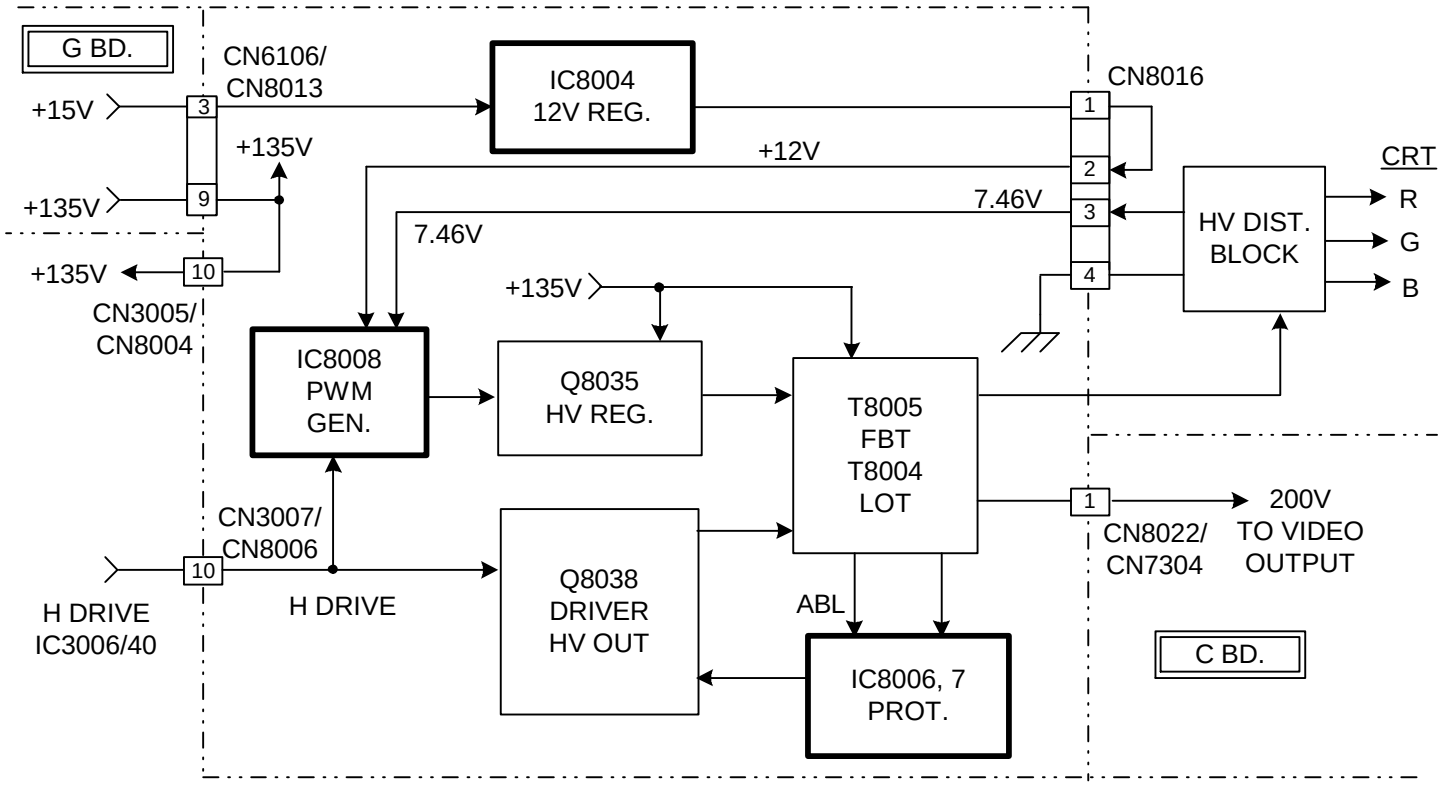


FIGURE 21-1 - RA-5 HV BLOCK

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Chart 21-2 explains the function of each block in the HV stage.

Chart 21-2 - HV Block Operation		
Block Name	Major component	Purpose
PWM Generator	IC8008, Q8035, Q9035	Provides regulated B+ supply voltage to the HV Output stage, preventing picture width fluctuations. A sample of the HV from the distribution block is used for error correction
LOT – Low Output Transformer	T8004	Primary is regulated voltage. Secondary outputs 200V B+ voltage to the RGB video output ICs on the C boards.
HV Drive / Output, FBT	Q8005, Q8032, Q8038, T8005	Amplifies the H drive signal to feed the flyback (FBT). The FBT develops the HV.
HV Distribution Block		Input is HV from the FBT. Outputs are HV for each CRT and one HV sample voltage reduced to about 7.4Vdc for regulation.
HV Protection	IC8006-7	Monitors the FBT output and stops the HV by grounding out the H Drive input.

Refer to Figure 21-2 for the operational description of the HV stage.

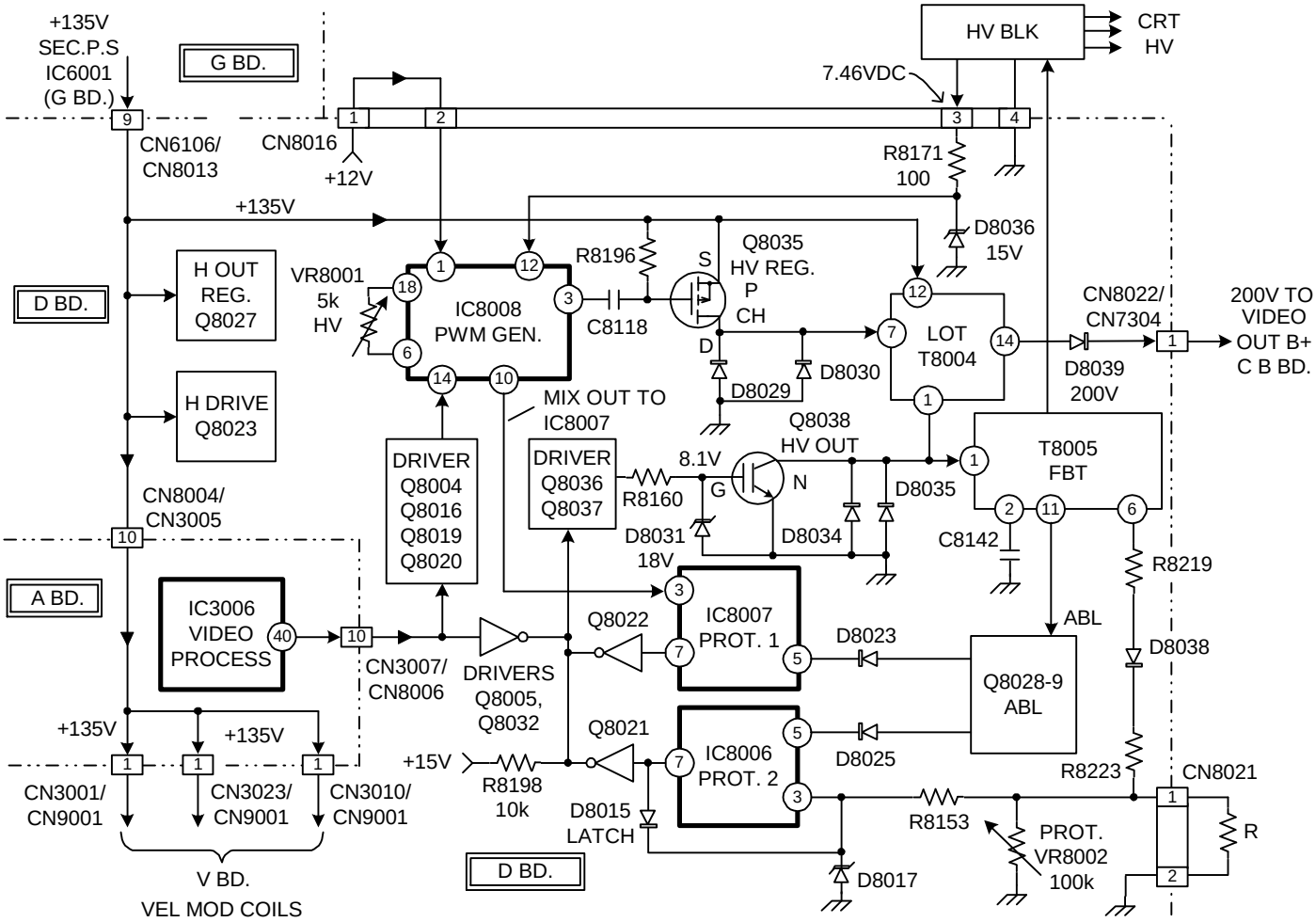


FIGURE 21-2 - HIGH VOLTAGE STAGE - RA-5 CHASSIS 34TVP12 1350 8/31/01

PWM Regulator

This stage controls the HV level by regulating the B+ voltage from Q8035. IC8008 starts when both 12Vdc and H drive pulses are input to pins 1 and 14 respectively. Pulses are output pin 3. The width of the pulse is dependent upon the error voltage input IC8008/pin 12. The higher the input voltage, the narrower the low going output pulses.

The pulses are amplified by P channel MOSFET Q8035 and applied to the primary winding of LOT T8004/pin 7. Typical voltage output from Q8035/drain = 130Vdc. The other end of this primary winding at pin 1 goes to HV Output Transistor Q8038/collector to develop HV. The secondary of LOT T8004 makes 200V for the RGB output drivers on the C boards (unrelated to the HV development but linked to maintain picture brightness uniformity).

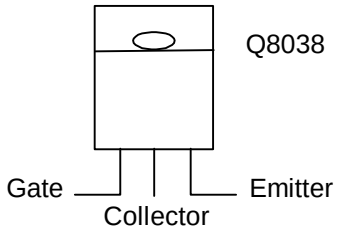
HV Drive / Output, FBT

This stage is located in Figure 21-2 below the PWM Regulator stage. It begins by amplifying the 33kHz horizontal drive signal from Video Process IC3006/pin 40 in various stages and uses the final amplified signal from Q8038 to drive the flyback transformer T8005. The flyback steps up the input voltage to HV level and the HV distribution block (external to the D board) sends the voltage to the three picture tubes. Another secondary winding of T8005/ pin 6 produces a low voltage that represents the FBT output. This output is rectified by D8038 and used in the HV protection circuit.

Q8038 is a new device used in this TV set. It tests like an enhancement N channel MOSFET. Normally, all leads measure infinity resistance to each other. If you charge the base/gate lead, then connect the ohmmeter + to the collector/drain, a resistance will appear for over an hour if the gate lead is not touched.

The test procedure for Q8038 is:

1. Check all leads of the device with respect to each other. Normal is no resistance (infinity).
2. Connect the negative lead of the ohmmeter (set to read diodes) to the emitter.
3. Touch the positive lead of the ohmmeter to the gate/base lead.
4. Move the positive lead of the ohmmeter to the collector/drain for a reading if Q8038 is OK.



Protection

The protection circuit grounds out the H drive signal to the HV stage, stopping the HV, which causes a dark screen but the sound remains normal.

These conditions will trip the protection circuit:

- Instructed to by regulator IC8008/pin 10 = HIGH (normally LOW).
- ABL from FBT/pin 11 goes LOW (caused by excessive pix tube current usually from shorted RGB Drivers).
- FBT output voltage rises to a critical threshold (T8005/pin 6).

These three inputs to Op Amps IC8006 and IC8007 form the protection circuit. When protection is called for, Pin 7 of either IC that was triggered goes HIGH. The HIGH is inverted by Q8021 or Q8022. Either transistor turning on will ground out the H Drive signal that feeds HV Output Q8038. That stops the HV.

What keeps the HV latched ON until the TV is shut down is D8015. When IC8006/pin 7 goes HIGH, this high is returned to the + input of the Op Amp at pin 3, keeping its output HIGH as long as power is applied. There is a similar latching diode connected across IC8007/pins 7 – 3 but not shown in Figure 21-2.

Testing for Dark Screen

A dark screen with normal sound can be caused by the items listed in Chart 21-3. Use Figure 21-3 of the D board in conjunction with Chart 21-3 to locate the test points.

Chart 21-3 – Common Causes of a Dark Screen			
Cause	Board	Reason	Troubleshooting Procedure
Screen voltages too low	Screen adj. on Chassis	IK blanking brings all CRT cathodes high if a screen voltage is low	1. Look at each CRT. If there is an IK line at any CRT, there is HV and deflection. If there is a line missing, CRT drive is missing from the A board. 2. The screen control is above the speakers. Turn one at a time until retrace lines appear then back off 3. Check for a sample of the HV at CN8016/pin 3 =7.46Vdc if the HV is normal. 0V if there is no HV.
Video blanking	A, B	RGB cathode voltages stay abnormally high at 200Vdc	
No HV	D, A, or G	No HV or too low.	

Figure 21-3 - D Board

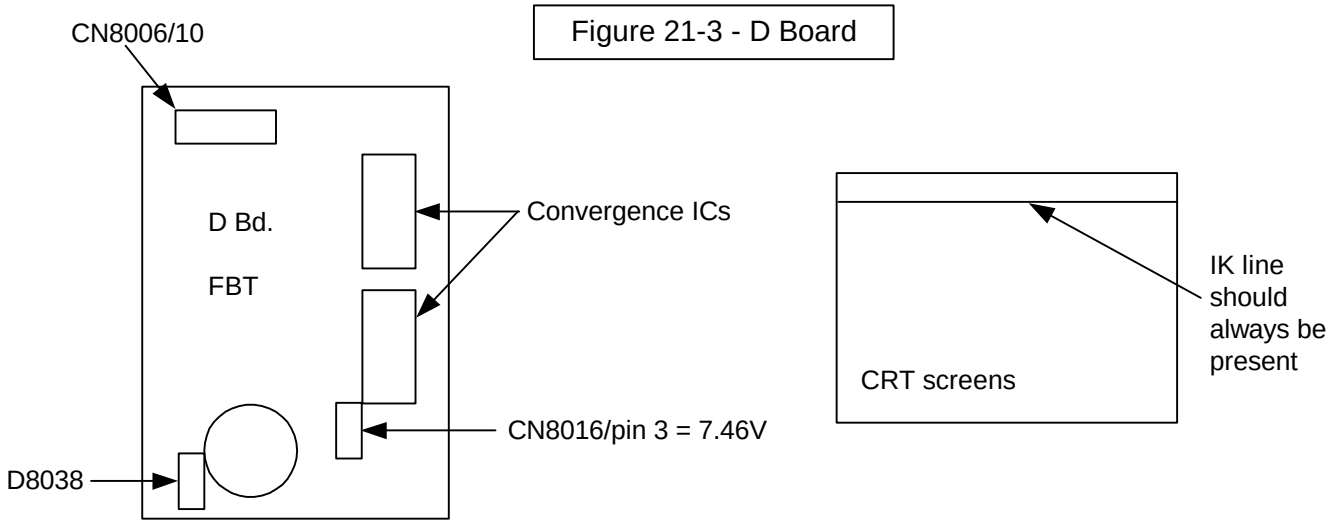


Figure 21-4 provides the step-by-step troubleshooting procedure. Refer to Figure 21-3 for test point location.

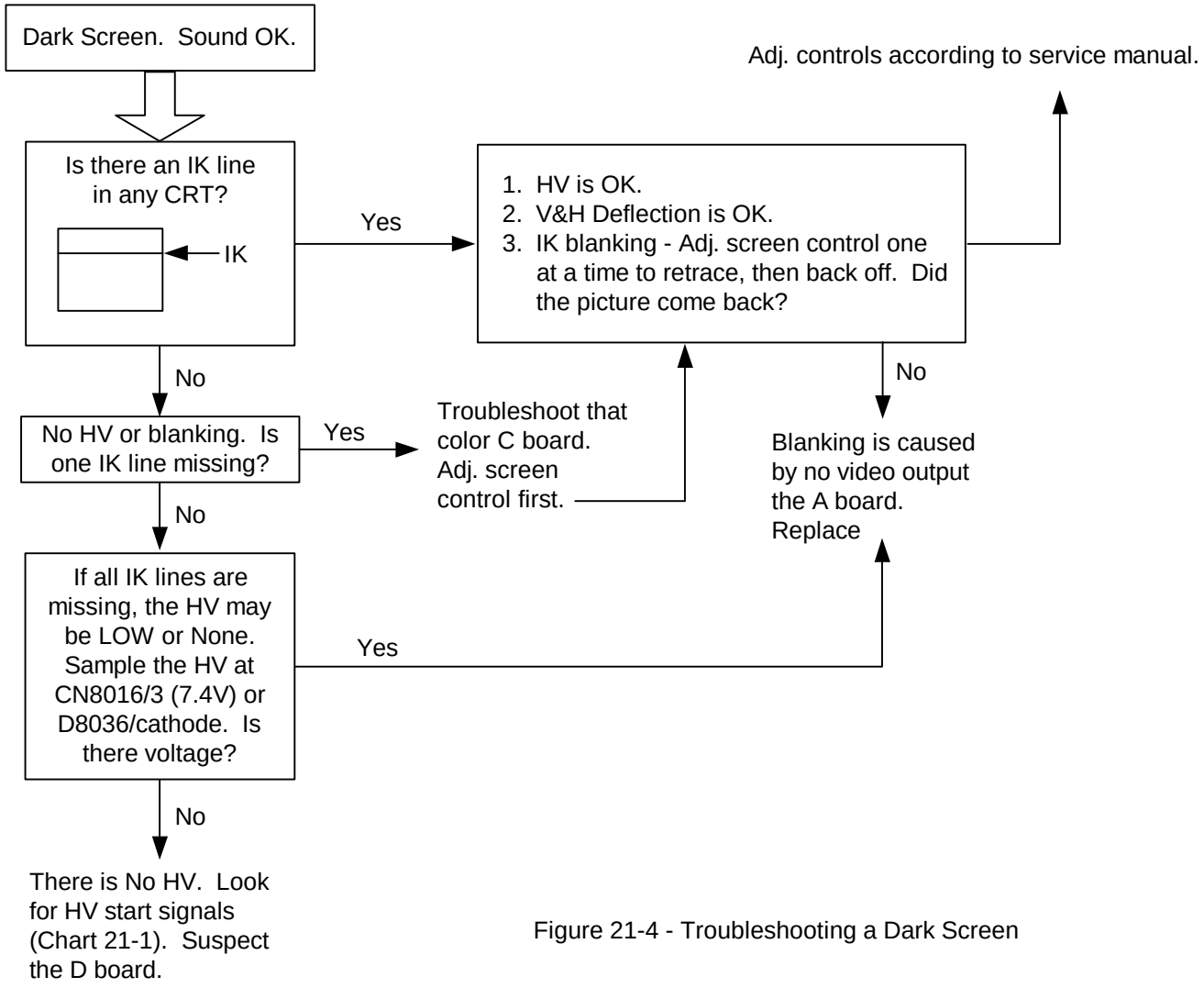

Dark Screen. Sound OK.
Is there an IK line in any CRT?
IK
Yes
1. HV is OK.
2. V&H Deflection is OK.
3. IK blanking - Adj. screen control one at a time to retrace, then back off. Did the picture come back?
Adj. controls according to service manual.
No
No HV or blanking. Is one IK line missing?
Yes
Troubleshoot that color C board. Adj. screen control first.
No
Blanking is caused by no video output the A board. Replace
No
If all IK lines are missing, the HV may be LOW or None. Sample the HV at CN8016/3 (7.4V) or D8036/cathode. Is there voltage?
Yes
No
There is No HV. Look for HV start signals (Chart 21-1). Suspect the D board.

Figure 21-4 - Troubleshooting a Dark Screen

Video Process (RA-5A Chassis)

The Video processing for the projection TV chassis is almost identical to the HA-3 chassis. The difference is the A board. An AD board is a plug-in to the A board for convergence operation and the output connector is a different number. Refer to Figure 22-1 of the RA-5A overall video block diagram for the following description of the similarities and differences and Figure 22-2 for the location of the video and sync signal checkpoints.

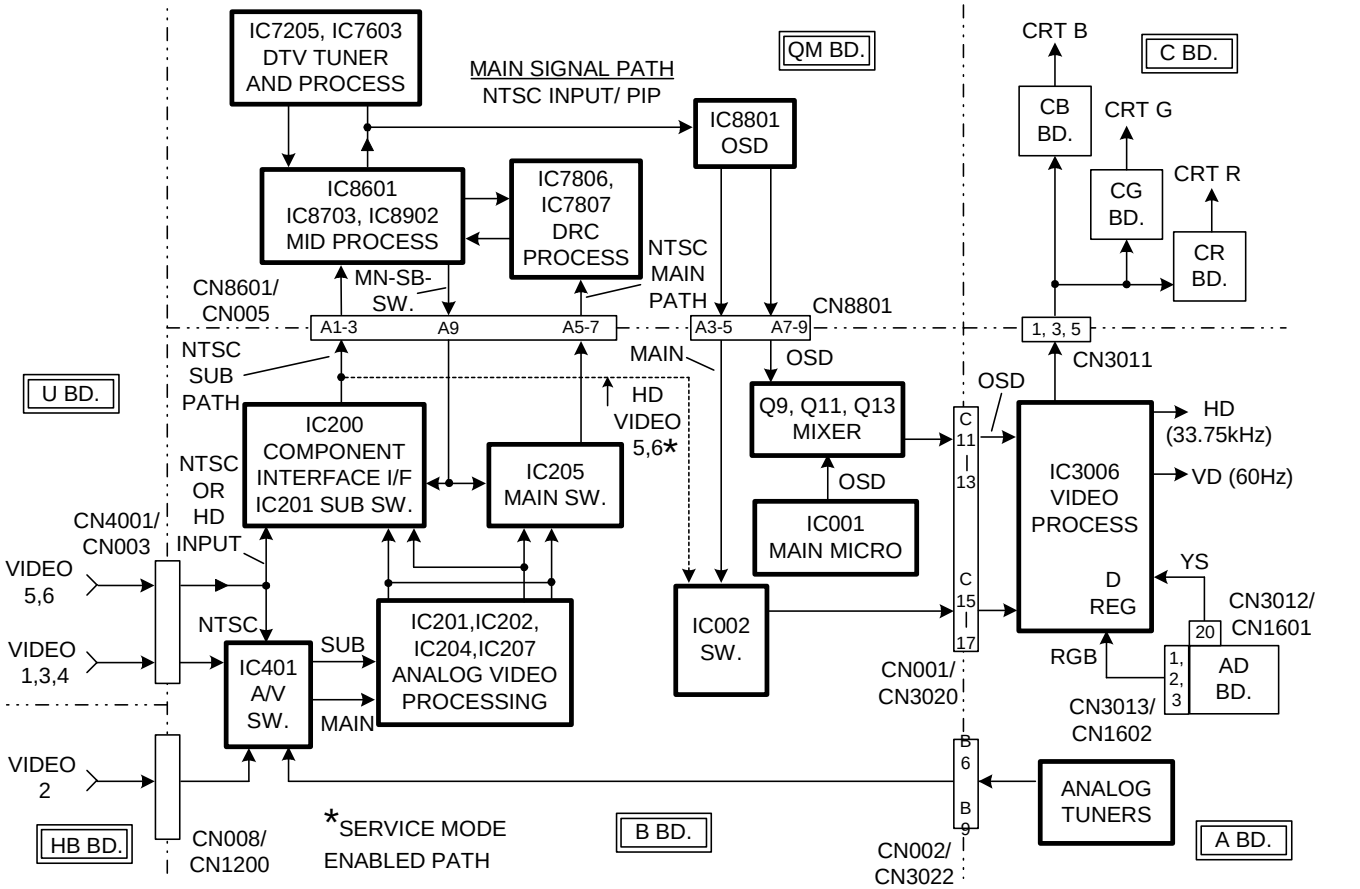


FIGURE 22-1 - VIDEO BLOCK - RA-5 CHASSIS 48TVP12 1360 9/4/01

HA-3 / RA-5A Similarities

The HA-3 TV chassis and RA-5A TV chassis share an almost identical QM and B board with minor differences to the NVM software so they are not interchangeable. Refer to the service manual for the board's part number and you will see they are stocked independently for ease of servicing. The signal flow between these boards is identical so you may refer to the previous Video Process description in the HA-3 section of this training manual.

HA-3 / RA-5A Differences

The A board is very different between these two sets. The two differences that pertain to the video section are shown in Figure 22-1:

- IC3006 was labeled the Y/C CRT Drive in the HA-3 chassis, but is labeled "Video Process (or)" here.
- The single CN3011 RGB output connector branches out to three CRTs simultaneously. The RGB signal wires from CN3011 go directly to their corresponding CRT board. In previous projection TV sets, the RGB signals passed through the C boards in series
- The projection TV's A board has a plug-in registration (convergence) AD board. This board produces either video patterns for Flash Focus or crosshatch patterns for convergence (service mode only). When a pattern is called for, Main Micro IC001 sends a request (data path not shown) to the micro in the AD board.

The AD board generates the pattern as an RGB signal (CN3013/pin 1-3) that is sent to Video Processor IC3006 (A board). The RGB pattern is accompanied by a Ys switching signal from CN3012/pin 20. The Ys control signal from the AD board is normally 0Vdc, but goes to 5Vdc when the Flash Focus pattern or convergence pattern is called for. See Chart 22-1.

Chart 22-1 - Video Process(or) Output Vs Ys control Input	
Picture Output	Ys input from CN3012/pin 20 AD board
Normal picture	0Vdc
Flash Focus or Convergence crosshatch	5Vdc

The 5Vdc Ys input signal tells IC3006 to replace the normal video path with the RGB pattern from the AD board when HIGH. This also implies that a defect on the AD board can stop the normal picture and leave a blank screen. The PJ TV set will still run normally <u>without</u> the AD board plugged in.

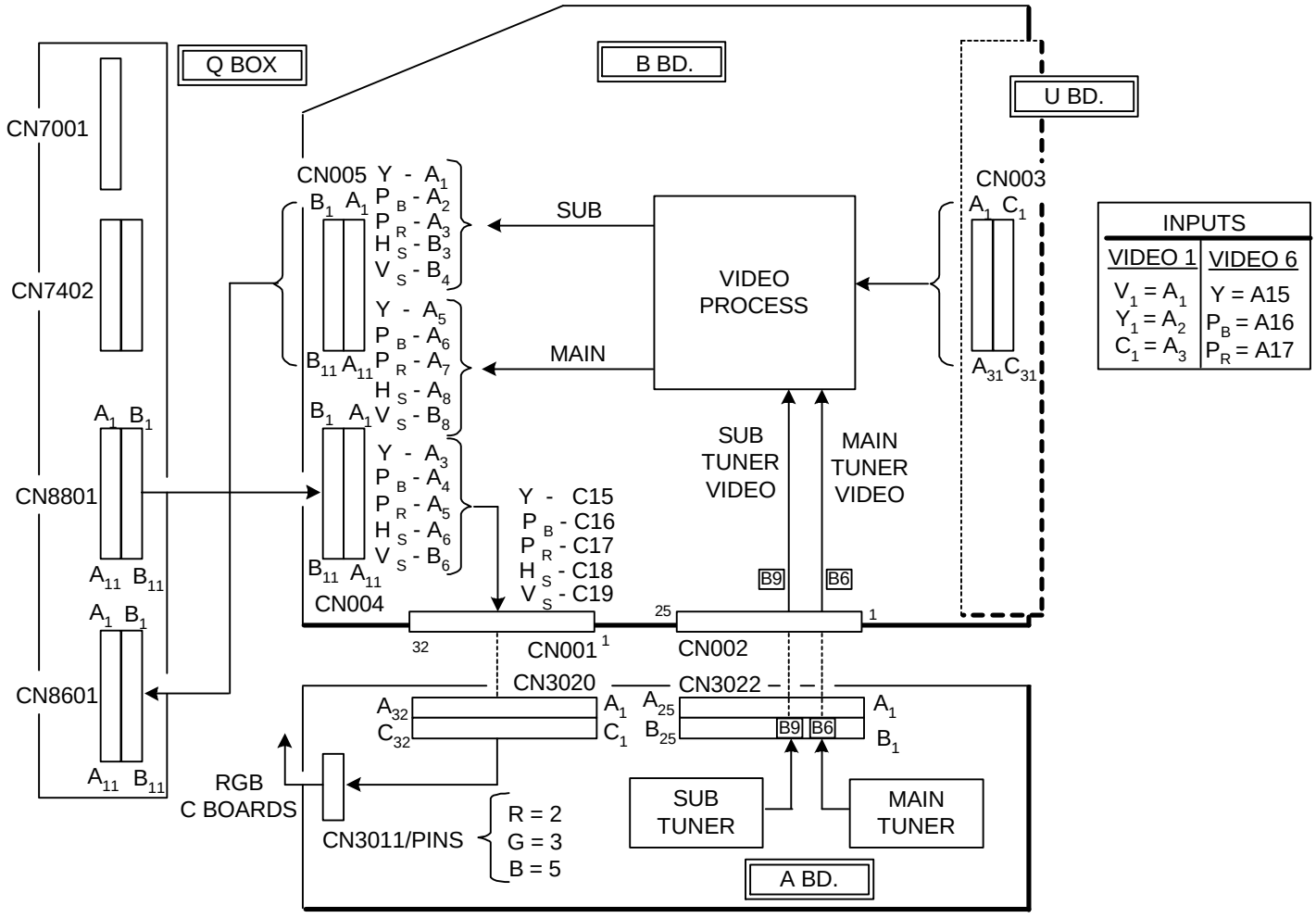


FIGURE 22-2 - PHYSICAL VIDEO/SYNC PATH (RA-5A CHASSIS) 50TVP12 1363 9/4/01

RA-5A Chassis Board Replacement

Board	Circuits	Fuses	Zeners	After board replacement
A	CRT (RGB) Driver H & V Oscillators/Jungle Both analog Tuners Deflection NVM IC3013 Shading circuit Flash focus buffers Audio output	R3024-IC3002-9Vreg R3077-neg15V line	D3001-33V – tuner D3004-5.1V-IC3006/56 protect D3006-5.6V-Stby 5V OVP D3025-5.6V- Stby 5V OVP	Transplant memory IC3013 containing deflection parameters.
AD	Convergence Processing Flash Focus sensing and processing		Flash Focus sensor signal protection-D1604-07. D1602-5V-5Vline OVP D1608-3.6V-3.3V line OVP	Complete convergence or transplant memory IC1607 containing convergence data and do touch up convergence.
B	Video processing and audio switching. Closed caption/V Chip Main Micro IC001 OSD (Menu)	None	None	Transplant memory IC004 containing system and user data. ** see note below chart
CR, CG, CB	RGB CRT signal amplifiers	None	None	No adjustments
D	HV Regulator circuit HV Flyback H Output Reg circuit H. Drive & H. Output V Output Two Convergence Amp packages (fused) Dynamic Focus Output	R8208=200V line (video out) PS8007=3A-CRT filaments PS8001=6-3A-Conv Output R8205-6=H centering (global)	D8028, D8038-HV Reg, Out protect D8036=HV Reg IC8008 protect D8024=15V-H. Out protect D8002-3=±15V protect-Vert Out D8026=5.6V fdbk H. pulse limiter	Adj Focus (on FBT). After ½ hour warm up, enter the service mode*, select category “PJE” (2 or #5 buttons) and perform touch up convergence adjustments. Adj. HV VR8001, 2 for HV level and shutdown according to safety related adj. in the service manual.

Board	Circuits	Fuses	Zeners	After board replacement
G	Standby Power Supply Primary Power Supply (Sub 6.5V, 11V, 7V.) Secondary Power Supply (135V, 22V, 19V, 15V) Protection latch circuit	F6001-10A-main R6099-Prim PS R6041-Sec PS PS6101-04=135V, ±22V, ±15V lines R6057-Stby PS R6073, R6081-2-Pri & Sec PS sustaining volt.	D6016=AC input OVP D6121, D6126=15V OVP, 22VOCP D6133=Sub 6.5V OVP	No adjustments
K	Prologic Decoding Audio Output Amplifiers Tone Control Pwr On/Off/Ch change mute	None	S Data protect D2301, D2303, D2305 S Clk protect D2302, D2304, D2306 Surround spk protection-D2602-5 Center Spk protection-D2619-20 Main spk protection-D2614-17 Var/Fixed output protection D2624-31	No adjustments
Q Box (Qi, QM Bds)	DRC for line doubling MID for twin pictures DTV Tuner and A/V process	None	D7803-3.9V=Reg for write PLL IC7805 (QM Bd)	Enter the service mode and check the model ID category items to see if they agree with the service manual. ** see note.
U	Audio/Video Input/output panel	None	None	No adjustments
V	Velocity Modulation	None	None	No adjustments

* Service Mode access using remote buttons: Display, #5, Vol +. Power. See the Convergence Adjustment Overview chapter for more information on the service mode.

** After replacing the B board or Q box you will find that the plugs to CN8801 and CN8601 are the same. Cables from Q box to CN004 and CN005 should cross. See Figure 23-1.

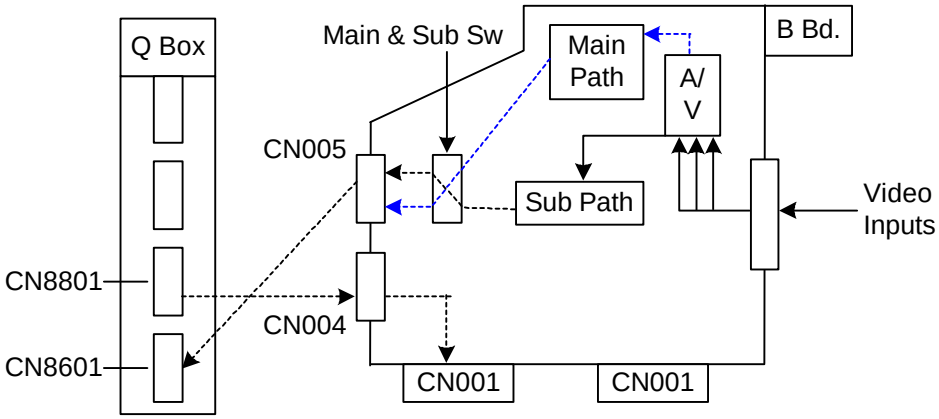
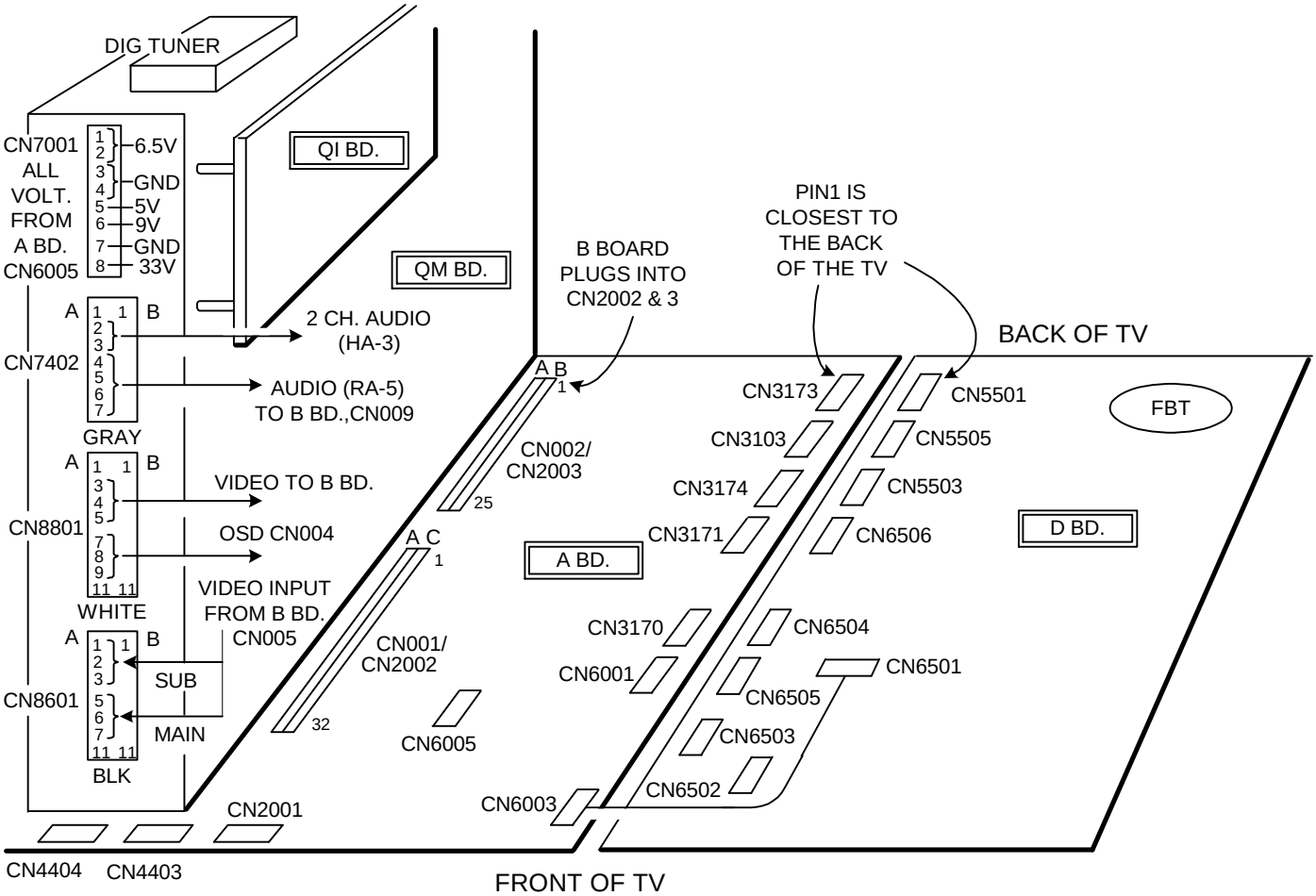


Figure 23-1 - HA-3 & RA-5A Video Path

NVM Contents – Chart 23-1

Chart 23-1 - TV's Non Volatile Memory (NVM) Contents			
B board IC004	A board IC3013	AD board IC1607	QM board IC7206 and IC8901
Active Analog & **Digital** TV stations & last channel/video	Deflection parameters (raster not video)	Convergence data	Picture parameters such as size position, etc (video not raster)
User Picture / Audio settings	CRT Drive settings	Flash Focus data	Single and Twin pix parameters
User Operation settings (DRC)			Freeze pix settings
Closed caption			
Service mode model ID			

APPENDIX



HA-3 CHASSIS CONNECTOR LAYOUT

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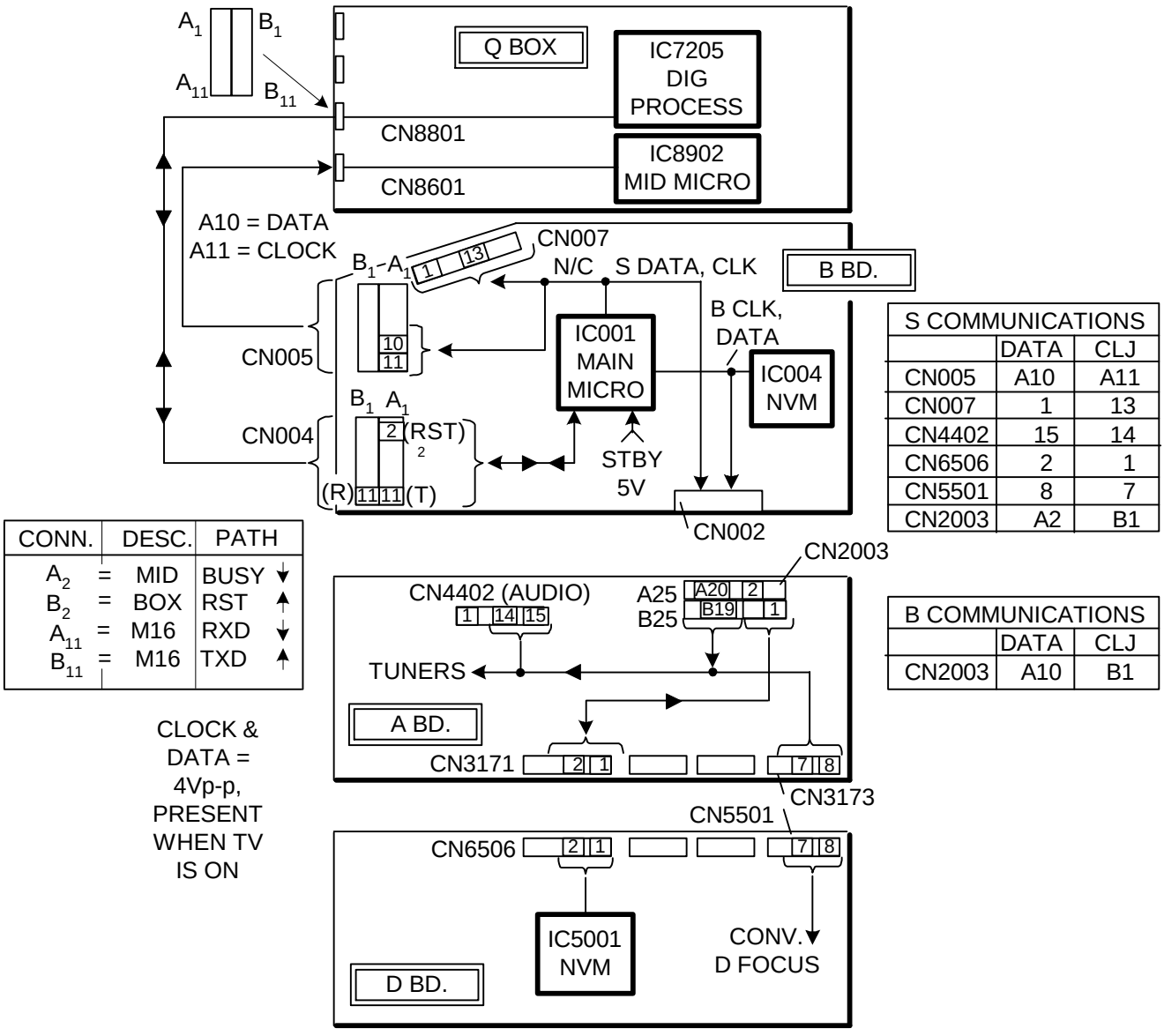

S COMMUNICATIONS		
	DATA	CLJ
CN005	A10	A11
CN007	1	13
CN4402	15	14
CN6506	2	1
CN5501	8	7
CN2003	A2	B1

B COMMUNICATIONS		
	DATA	CLJ
CN2003	A10	B1

HA-3 CHASSIS COMMUNICATION

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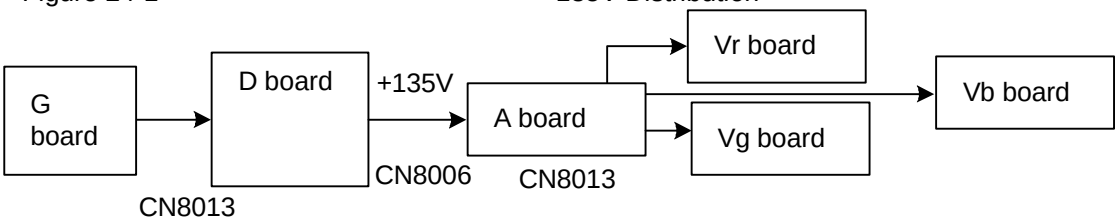
RA-5A Chassis D Board Tests

Many voltages from the G board are delivered to the D board (CN8013 in Figure 24-1) for deflection use. The 135V path continues into the A and V boards. A short on the D board will load down the power supply, but the D board can be quickly tested for shorts.

Figure 24-1 -135V Distribution

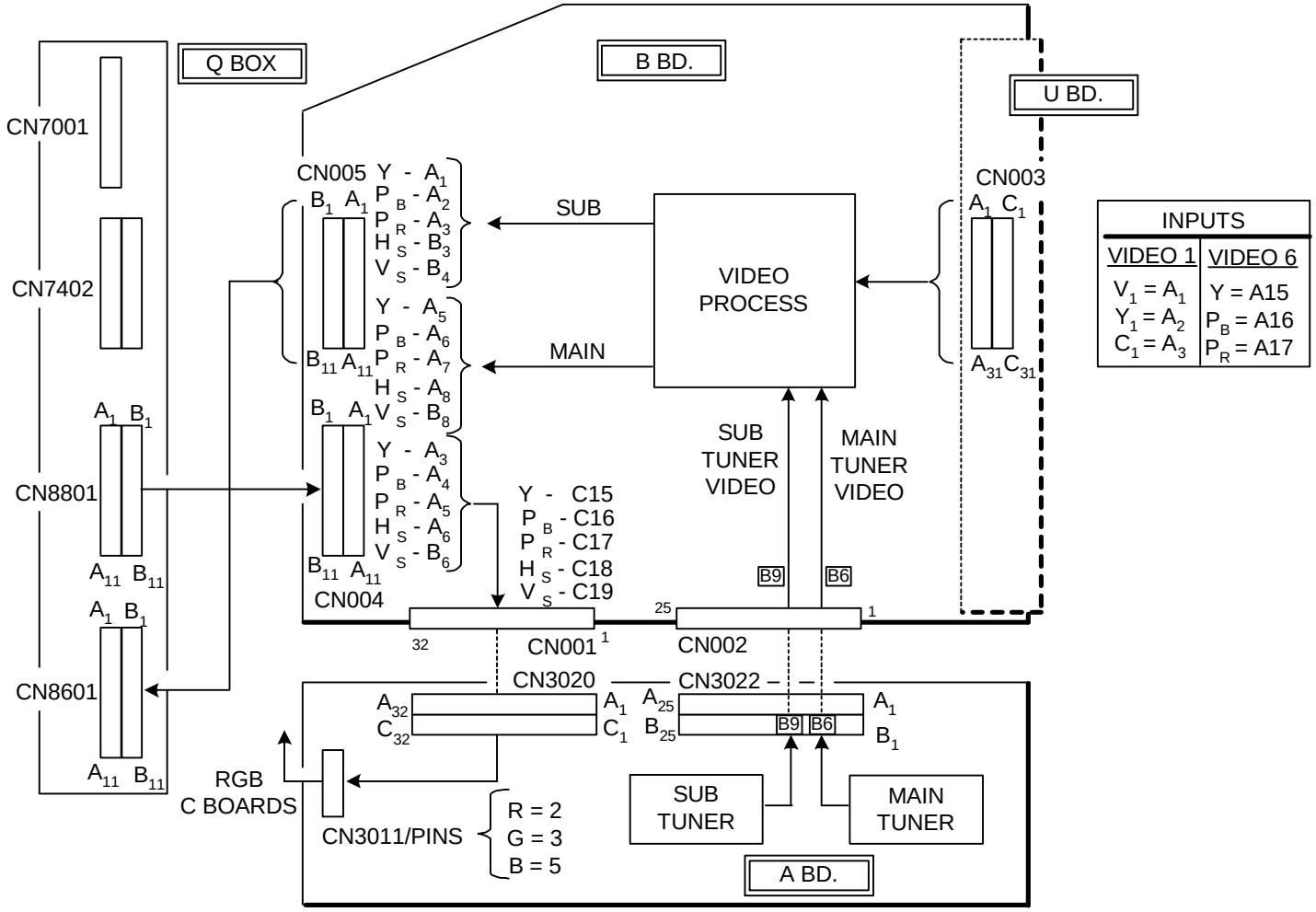


This D board can be tested for excessive current demand (shorts) either by making resistance (ohms) checks or by supplying voltage to each input of CN8013 to see if it is normal. The conditions are that the D board is unplugged from the TV before resistance measurements are taken and the polarity of the ohmmeter voltage matches that of the load. The DVM used was a Fluke 8050A set to 200k ohm range. Your ohmmeter will show different readings but they will be proportional.

The DVM leads were reversed so the – voltage from the DVM was applied to the –22 and –15 volt pins of CN8013/pins 1 and 4. By maintaining the correct polarity, premature parts failures can be avoided. See Chart 24-1.

Chart 24-1 - D Board Excessive Current Demand Tests

Input Name	Location	Ohms to Gnd (charging caps)	Current	Destination	Major Part
+135V	CN8013/pin 9	1.2k to 55k in 1 min.	0.5A at 30Vdc	HV Conv., PS for HV Conv, H Out, PS for H Out, A board	Q8038, Q8035, Q8024, Q8027, CN8006/10
+22Vdc	CN8013/pin 6	4k to infinity	0.02ma at 22Vdc	STK Convergence Amp, Dynamic Focus	IC8001, 2; Q8008, 9
-22Vdc	CN8013/pin 4	1.7k to 7k	9.29ma at –22Vdc		
+15Vdc	CN8013/pin 3	800 to 10.5k in 1 min	110.7ma at 15Vdc	Vertical Output H Drive	IC8003, Q8036, 7
-15Vdc	CN8013/pin 1	1k to 65k in 1 min.	5.09ma at –15Vdc		



PHYSICAL VIDEO/SYNC PATH (RA-5A CHASSIS)

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